BECKHOFF New Automation Technology

Original Manual for | EN

CB3067

Computerboard

30.03.2023 | Version: 1.2

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1 Documentation issue status

Version	Modifications
0.1	First preliminary version, G0
1.0	First release G2, with current BIOS 0.13 and new title page
1.1	G2, BIOS Version a.020 added
1.2	Information for real-time applications added

2 Notes on the documentation

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with applicable national standards.
It is essential that the documentation and the following notes and explanations are followed when installing and commissioning the components.
It is the duty of the technical personnel to use the documentation published at the respective time of each installation and commissioning.

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.

Disclaimer

The documentation has been prepared with care. The products described are, however, constantly under development.
We reserve the right to revise and change the documentation at any time and without prior announcement.
No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

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Patent Pending

The EtherCAT Technology is covered, including but not limited to the following patent applications and patents:
EP1590927, EP1789857, EP1456722, EP2137893, DE102015105702
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3 Safety instructions

Safety regulations

Please note the following safety instructions and explanations!
Product-specific safety instructions can be found on following pages or in the areas mounting, wiring, commissioning etc.

Exclusion of liability

All the components are supplied in particular hardware and software configurations appropriate for the application. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH & Co. KG.

Personnel qualification

This description is only intended for trained specialists in control, automation and drive technology who are familiar with the applicable national standards.

Description of symbols

In this documentation the following symbols are used with an accompanying safety instruction or note. The safety instructions must be read carefully and followed without fail!

⚠ DANGER

Serious risk of injury!

Failure to follow the safety instructions associated with this symbol directly endangers the life and health of persons!

⚠ WARNING

Risk of injury!

Failure to follow the safety instructions associated with this symbol endangers the life and health of persons!

⚠ CAUTION

Personal injuries!

Failure to follow the safety instructions associated with this symbol can lead to injuries to persons!

NOTE

Damage to the environment or devices

Failure to follow the instructions associated with this symbol can lead to damage to the environment or equipment.

Tip or pointer

This symbol indicates information that contributes to better understanding.

UL note

This symbol indicates important information regarding UL certification.

Intended use

The CB3067 Computer Board was designed and developed exclusively for configuration in automation processes. To that end the board is equipped with external interfaces in order to acquire or output digital or analog signals or forward them to higher-level components.

Any other use is regarded as inappropriate.

The specified limits for electrical and technical data must be adhered to.

4 Overview

4.1 Properties

The CB3067 is a highly complex 3.5-inch board. It is based on Intel®'s Coffee-Lake S-processors of the Core™, Celeron™ and Pentium families in conjunction with the Q370 chipset.

State-of-the-art, energy-saving DDR4 technology enables a memory extension of up to 64 GB (DDR4-2666) using SO-DIMM260. In addition to a PCI-Express bus, further peripheral devices are available, such as HDMI or DisplayPort via I-PEX, 4x SATA with up to 6 Gbit/s, DVI/HDMI, 11x USB (of which 5x USB 3.0), 2x Gbit-LAN, and an external and an internal serial interface.

The input voltage is 5 V.

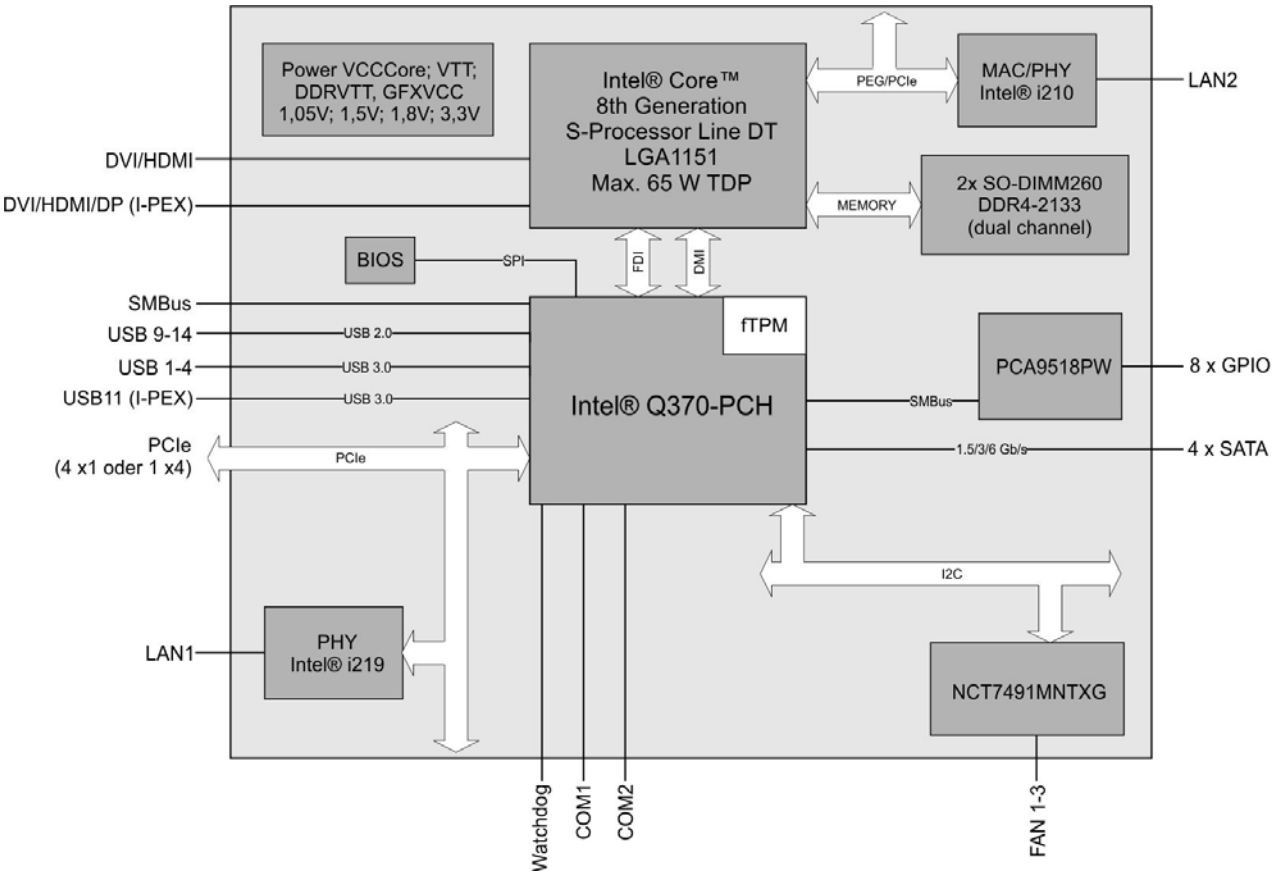


Fig. 1: CB3067 block diagram

4.2 List of features

CB3067	3.5-inch board
CPU	Intel® Core™ i3/Core™ i5/Core™ i7 Intel® Pentium® Intel® Celeron®
Chipset	Intel® Q370-PCH
Memory	2x SO-DIMM260 1.2 V DDR4-2666 Maximum memory extension 64 GB
I/O external	1x DVI-D (DVI or HDMI 1.4) 2 x Gbit LAN, Intel® i219 and i210 4x USB3.0 1 x COM A
I/O internal	1x I-PEX (HDMI1.4 or DP1.2 and USB 3.0) 4x SATA 3.0, RAID 0/1/5/10 1x PCIe Gen3 (1x PCIe x4 or 4x PCIe x1) 6x USB 2.0 8x GPIO 1 x COM B
Graphic resolution	DisplayPort: 4096x2304@60 Hz HDMI1.4: 4096x2304@60 Hz 4096x2160@24 Hz DVI: 1920x1200@60 Hz
RTC	External CMOS battery
BIOS	AMI® Aptio V
Power supply	5 V/S5 V/3.3 V/12 V
Format	102 x 147 mm

Availability of the processors

The list of features lists all the processors that can be ordered. Their actual availability depends on the manufacturer.

4.3 Specifications and documents

The following documents, specifications or webpages were used for the preparation of this manual or as further technical documentation respectively.

- **PCI specification**
- Version 2.3 or 3.0
- www.pcisig.com
- **PCI Express® Base Specification**
- Version 5.0
- www.pcisig.com
- **ACPI specification**
- Version 5.0
- www.acpi.info
- **ATA/ATAPI specification**
- Version 7 Rev. 1
- www.t13.org
- **USB specifications**
- www.usb.org
- **SM-Bus specification**
- Version 2.0
- www.smbus.org
- **Intel® chip descriptions**
- Intel® Core™ processor product family data sheet
- www.intel.com
- **Intel® chip description**
- I219 data sheet
- i210 datasheet
- www.intel.com
- **SMSC® chip description**
- SCH3114 datasheet (NDA required)
- www.smsc.com
- **American Megatrends®**
- Aptio™ Text Setup Environment (TSE) User Manual
- www.ami.com
- **American Megatrends®**
- Aptio™ 5.x Status Codes
- www.ami.com

5 Detailed description

5.1 Power supply

The connection for the power supply of the CB3067 is implemented as a 2x10-pin housing connector.

The 12 V supply is required for the operation of PCI-Express cards and the fan connections. COM RXD and TXD can also be used for your own power supply unit, e.g. for the UPS function.

Communication takes place via SMBus (SMB-CLK/SMB-DAT).

NOTE

Use only a Beckhoff-certified power supply unit!

The CB3067 is intended exclusively for operation with the Beckhoff CA2000-0026 power supply unit, as only in this way can the 3.3 V supply be guaranteed.

5.2 Second UPS

The CB3067 can optionally be equipped with a plug-in second UPS, which can maintain the supply of power for a few seconds, depending on its capacitance and the current consumption of the board, in order to compensate brief power failures or voltage fluctuations. The maximum capacitance is limited by the space requirement.

NOTE

Do not use the rechargeable battery and the second UPS simultaneously!

The CB3067 can be operated either with a rechargeable battery or with a second UPS module. To avoid data loss in case of a power cut, the two components may not be used simultaneously!

5.3 CPU

The processors used are the 8th and 9th generation of Intel®'s Coffee-Lake S-CPUs from the Core™, Pentium™ and Celeron™ families. The processors of both generations are characterized by very low power consumption and offer contemporary performance with clock rates of currently up to 4.4 GHz.

The Intel® processors from the Coffee-Lake family have an extended ambient temperature range and are therefore particularly suitable for use in industrial systems.

5.4 Memory

SO-DIMM260 memory modules (DDR4-2666), as commonly used in notebooks, are used on the CB3067 board. For technical and mechanical reasons, it is possible that certain memory modules cannot be used. Information regarding the recommended memory modules can be obtained from your distributor.

Depending on the product version, a memory extension up to 32 GB is possible with the currently available SO-DIMM260 modules.

Population of both memory slots

When populating both memory slots, make sure that you use identical memory modules.

6 Connections

All the connectors on the CB3067 are described on the following pages.

Requirement for the cabling!

The cables used must meet certain requirements for most interfaces. For example, twisted and shielded cables are necessary for a reliable USB 2.0 connection. Limitations in the maximum cable length are also no rarity. All of these interface-specific requirements can be found in the respective specifications and you should observe them accordingly.

6.1 Plug connector overview

The illustration below shows the plug connections on the component side of the CB3067 board. The function of the respective connector can be taken from the table below. The listed page in the manual provides you with further information on this connection. The interfaces are described clockwise, beginning with the power input (P1300).

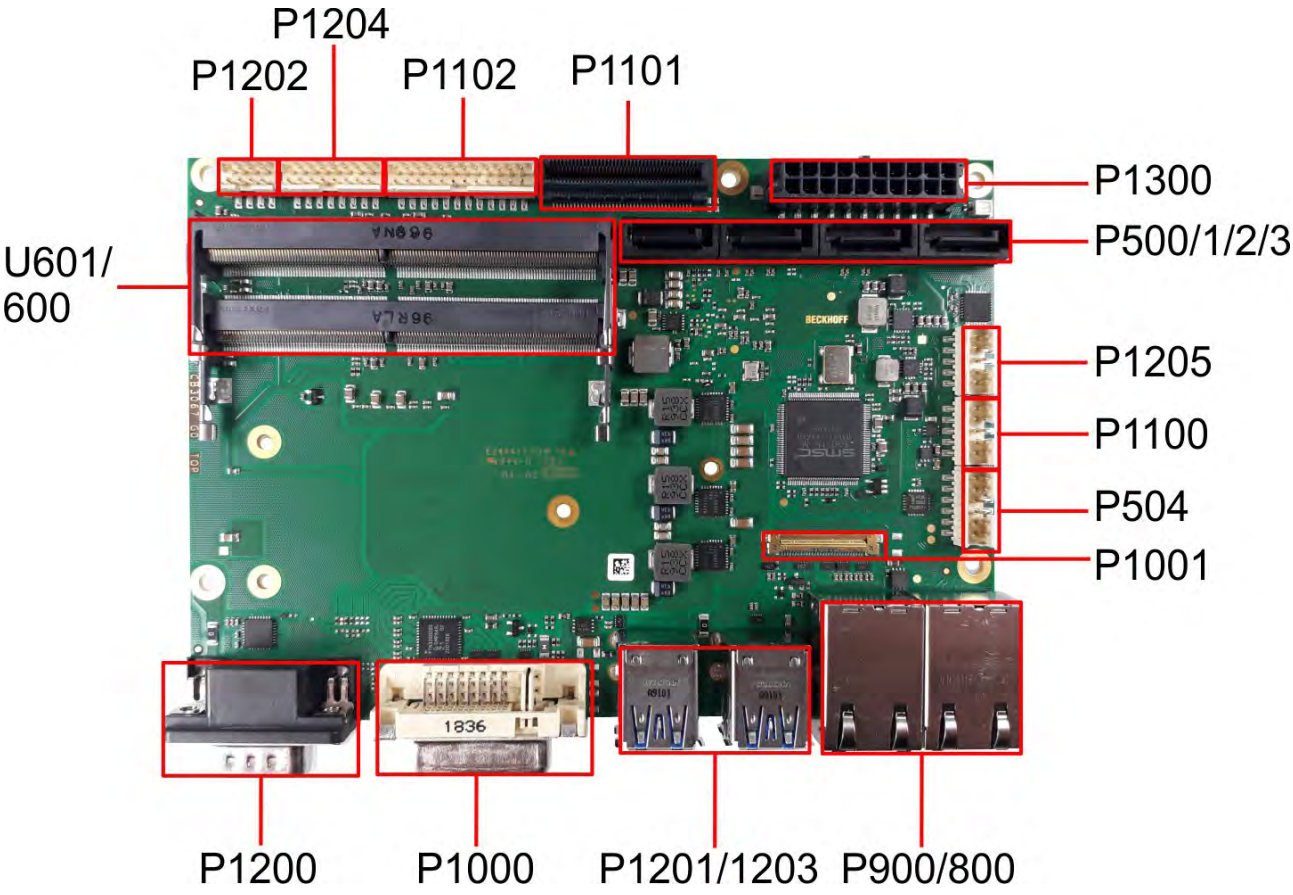


Fig. 2: CB3067 connector overview

Number	Function (designation)	Page
P1300	Power input	Power input (P1300) [▶ 15]
P500/1/2/3	SATA interfaces	SATA interfaces (P500/1/2/3) [▶ 16]
P1205	Serial interface, internal	Serial interface COM2 internal (P1205) [▶ 16]
P1100	Fan connection, internal	Fan connections (P1100) [▶ 17]
P504	GPIO	GPIO (P504) [▶ 17]
P1001	Display port IPEX	Display port IPEX (P1001) [▶ 18]
P800/900	1 Gbit LAN	LAN (P900/800) [▶ 19]
P1201/1203	USB 3.0	USB 3.0 external (P1201/P1203) [▶ 20]
P1000	DVI-D	DVI-D (P1000) [▶ 21]
P1200	COM A, external	Serial interface COM1 (P1200) [▶ 22]
U600/601	2 x SODIMM 260 DDR4	Memory SO-DIMM260 (U601/U600) [▶ 23]
P1202	2 x USB 2.0, internal	USB 2.0 internal (P1202/P1204) [▶ 27]
P1204	4 x USB 2.0, internal	USB 2.0 internal (P1202/P1204) [▶ 27]
P1102	System, internal	System connector (P1102) [▶ 28]
P1101	PCIe x4	PCI-Express connector (P1101) [▶ 29]

6.2 Power input (P1300)

The connection for the power supply of the CB3067 is implemented as a 2x10-pin housing connector.

The 12 V supply is required for the operation of PCI-Express cards and the fan connections. COM RXD and TXD can also be used for your own power supply unit, e.g. for the UPS function.

Communication takes place via SMBus (SMB-CLK/SMB-DAT).

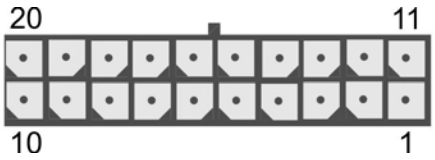


Fig. 3: CB3067 power input (P1300)

Pin assignment power input					
Description	**Name**	**Pin**		**Name**	**Description**
SMBus clock signal/ COM transmit data	SMB_CLK COM.TXD	1	11	SMB_DAT/ COM.RXD	SMBus data/ COM receive data
'Power Supply On' input for switching on the output voltages: Low (0 V) = switch on voltages High (5 V or open contact) = switch off voltages	PS_ON	2	12	ATX PWRGOOD	'ATX Powergood' output signals to the PC that all voltages are switched on: Low (0 V) = voltage not ok Open Drain = voltage ok
Power button output for switching the connected PC on and off	ATX PWRBTN#	3	13	S VCC	S5 V supply voltage
12 V supply voltage	12 V	4	14	12 V	12 V supply voltage
Ground	GND	5	15	GND	Ground
Ground	GND	6	16	GND	Ground
5 V supply voltage	VCC	7	17	VCC	5 V supply voltage
5 V supply voltage	VCC	8	18	VCC	5 V supply voltage
SUPS active output: Low (0 V) = SUPS inactive High (3.3 V) = SUPS active	SUSV	9	19	GND	Ground
3.3 V supply voltage	3.3 V	10	20	3.3 V	3.3 V supply voltage

6.3 SATA interfaces (P500/1/2/3)

The CB3067 board is equipped with four SATA interfaces, which allow a data transfer rate of up to 6 Gbit per second. The interfaces are available as 7-pin standard SATA connectors. RAID 0/1/5/10 are supported.

The necessary settings are made via the BIOS setup.

Fig. 4: CB3067 SATA (P500/1/2/3)

Pin assignment SATA interfaces		
Pin	**Name**	**Description**
1	GND	Ground
2	SATATX	SATA Transmit +
3	SATATX#	SATA Transmit -
4	GND	Ground
5	SATARX#	SATA Receive -
6	SATARX	SATA Receive +
7	GND	Ground

6.4 Serial interface COM2 internal (P1205)

The internal serial interface COM2 is implemented with a 2x5-pin connector. The signals are available according to the RS232 standard.

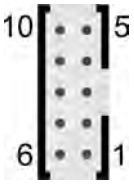


Fig. 5: CB3067 COM2 internal (P1205)

Pin assignment COM2 internal					
Description	**Name**	**Pin**		**Name**	**Description**
Data Carrier Detect	DCD	1	6	DSR	Data Set Ready
Receive Data	RXD	2	7	RTS	Request to Send
Transmit Data	TXD	3	8	CTS	Clear to Send
Data Terminal Ready	DTR	4	9	RI	Ring Indicator
Ground	GND	5	10	VCC	3.3 V supply voltage

6.5 Fan connections (P1100)

Three fans with a supply voltage of 12 Volt can be connected to the module. This takes place with a 2x5-pin connector. There are also signals for monitoring the fan speed.

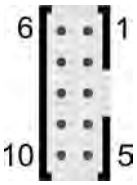


Fig. 6: CB3067 fan (P1100)

Pin assignment fan connection					
Description	**Name**	**Pin**		**Name**	**Description**
Fan 1 switched to ground	FANON1	1	6	FANON2	Fan 2 switched to ground
12 V supply voltage	12 V	2	7	12 V	12 V supply voltage
Fan 1 monitoring	FANCTRL1	3	8	FANCTRL2	Fan 2 monitoring
12 V supply voltage	12 V	4	9	FANCTRL3	Fan 3 monitoring
Fan 3 switched to ground	FANON3	5	10	GND	Ground

6.6 GPIO (P504)

The board has a general purpose input/output interface that is fed out via a 2x6-pin connector. By programming the associated chip (PCA9535BS) accordingly, I/O functions can be created here in a very flexible manner. Ask your distributor about appropriate software support

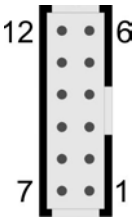


Fig. 7: CB3067 GPIO (P504)

Pin assignment GPIO					
Description	**Name**	**Pin**		**Name**	**Description**
5 V supply voltage	VCC	1	2	VCC	5 V supply voltage
GP input/output1	GPIO0	3	4	GPIO4	GP input/output5
GP input/output2	GPIO1	5	6	GPIO5	GP input/output6
GP input/output3	GPIO2	7	8	GPIO6	GP input/output7
GP input/output4	GPIO3	9	10	GPIO7	GP input/output8
Ground	GND	11	12	GND	Ground

6.7 Display port IPEX (P1001)

The CB3067 has a further DVI connection, which is implemented in the form of a 30-pin ribbon cable connector. There are no analog VGA signals on this connection, but an HDMI or DisplayPort screen can be connected. In addition, a further USB channel is fed out via this connector. This USB channel supports the specification 3.0. It supplies up to 900 mA current and is electronically protected.

When cabling, be sure to connect receive cables with transmit cables and vice versa. The current drawn from VCC must not exceed 2 A in total (0.5 A per contact); for 3.3 V, the maximum current is 1 A (0.5 A per contact).

NOTE

Use IPEX cables!

Use a special I-PEX cable for this interface.

Fig. 8: CB3067 Display Port IPEX (P1001)

Pin assignment Display Port IPEX		
Pin	**Name**	**Description**
1	TMDS0#/DP2#	DVI Data 0 - / DP Lane 2 -
2	TMDS0/DP2	DVI Data 0 + / DP Lane 2 +
3	TMDS1#/DP1#	DVI Data 1 - / DP Lane 1 -
4	TMDS1/DP1	DVI Data 1 + / DP Lane 1 +
5	TMDS2#/DP0#	DVI Data 2 - / DP Lane 0 -
6	TMDS2/DP0	DVI Data 2 + / DP Lane 0 +
7	TMDSCLK#/DP3#	DVI Clock - / DP Lane 3 -
8	TMDSCLK/DP3	DVI Clock + / DP Lane 3 +
9	N/C	Not connected
10	SEL_DVI/DP#	DVI-DisplayPort Select
11	DDCK/DPAUX	EDID Clock / DP Aux +
12	DDDA/DPAUX#	EDID Data / DP Aux -
13	VCC	5 V supply voltage
14	GND	Ground
15	HPD	Hot Plug Detect
16	USBVCC	USB supply 5 V
17	USBVCC	USB supply 5 V
18	N/C	Not connected
19	N/C	Not connected
20	SSRX-	SuperSpeed Receive -
21	SSRX+	SuperSpeed Receive +
22	USB-	USB minus data channel
23	USB+	USB plus data channel
24	SSTX-	SuperSpeed Transmit-
25	SSTX+	SuperSpeed Transmit+
26	3.3 V	3.3 V supply voltage
27	3.3 V	3.3 V supply voltage
28	VCC	5 V supply voltage
29	VCC	5 V supply voltage
30	VCC	5 V supply voltage

6.8 LAN (P900/800)

The board has two Gigabit-LAN connections. Network components compatible with 10BaseT, 100BaseT and 1000BaseT can be connected to both. The required speed is selected automatically. Auto-Cross and Auto-Negotiate are available as well as PXE and WOL functionality. Controllers are Intel®'s i219 (PHY, LAN1) and i210 (MAC/PHY, LAN2).

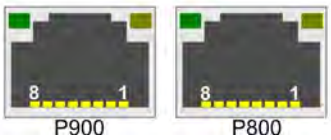


Fig. 9: CB3067 LAN (P900-800)

Real-time applications

The Ethernet port connected via PCIe is usually suitable for cycle times <= 1 ms and for distributed clock applications with EtherCAT.
The Ethernet port integrated in the chipset is usually suitable for real-time Ethernet applications with cycle times > 1 ms (without distributed clocks).

Pin assignment LAN					
Description	**Name**	**Pin**		**Name**	**Description**
LED LAN LINK/ACT	LINKACT 1	1	7	SPEED1000	LED LAN 1000MB
LAN line 1 plus	LAN11+	2	8	LAN10+	LAN line 0 plus
LAN line 1 minus	LAN11-	3	9	LAN10-	LAN line 0 minus
LAN line 3 plus	LAN13+	4	10	LAN12+	LAN line 2 plus
LAN line 3 minus	LAN13-	5	11	LAN12-	LAN line 2 minus
LED LAN 100MB	SPEED100	6	12	S3.3V	Standby supply voltage 3.3 V

6.9 USB 3.0 external (P1201/P1203)

USB 3.0 channels 1 to 4 are fed out in the form of standard USB connectors.

The USB channels support the USB specification 3.0. All necessary settings for USB can be made by the BIOS.

NOTE

Functionality of USB mouse and keyboard

Note that the "USB Mouse and Keyboard" functionality of the BIOS setup is only required if the operating system does not provide USB support. Do not select this function for settings in the setup and for booting Windows with a connected USB mouse and keyboard, because this would result in significant performance limitations.

The individual USB interfaces can supply a current of up to 900 mA and are electronically protected.

Fig. 10: CB3067-USB3.0 (P1201+1203)

Pin assignment USB 3.0		
Pin	**Name**	**Description**
1	VCC	5 V for USBX
2	USBX#	Minus data channel USBX
3	USBX	Plus data channel USBX
4	GND	Ground
5	StdA_SSRX-	SuperSpeed Receiver -
6	StdA_SSRX+	SuperSpeed Receiver +
7	GND	Ground
8	StdA_SSTX-	SuperSpeed Transmitter -
9	StdA_SSTX+	SuperSpeed Transmitter +

6.10 DVI-D (P1000)

The board has a DVI-D connection for DVI-capable displays. Analog displays cannot be connected.

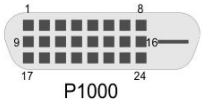


Fig. 11: CB3067 DVI-D (P1000)

Pin assignment of DVI-D		
Pin	**Name**	**Description**
1	TMDSDAT2#	DVI Data 2 -
2	TMDSDAT2	DVI Data 2 +
3	GND	Ground
4	N/C	Not connected
5	N/C	Not connected
6	DDCCLK	DDC Clock (DVI/VGA)
7	DDCDAT	DDC Data (DVI/VGA)
8	N/C	Not connected
9	TMDSDAT1#	DVI Data 1 -
10	TMDSDAT1	DVI Data 1 +
11	GND	Ground
12	N/C	Not connected
13	N/C	Not connected
14	VCC	5 V supply voltage
15	GND	Ground
16	HP_DETECT	Hot Plug Detect
17	TMDSDAT0#	DVI Data 0 -
18	TMDSDAT0	DVI Data 0 +
19	GND	Ground
20	N/C	Not connected
21	N/C	Not connected
22	GND	Ground
23	TMDSCLK	DVI-Clock
24	TMDSCLK#	DVI-Clock

6.11 Serial interface COM1 (P1200)

The COM1 serial interface is fed out via a 9-pin standard DSUB connector (male). The signals are available according to the RS232 standard.

The port address and the interrupt used are set with the help of the BIOS setup.

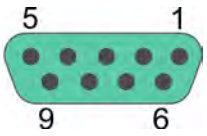


Fig. 12: CB3067 COM1 (P1200)

Pin assignment of COM1					
Description	**Name**	**Pin**		**Name**	**Description**
Data Carrier Detect	DCD	1	6	DSR	Data Set Ready
Receive Data	RXD	2	7	RTS	Request to Send
Transmit Data	TXD	3	8	CTS	Clear to Send
Data Terminal Ready	DTR	4	9	RI	Ring Indicator
Ground	GND	5			

6.12 Memory SO-DIMM260 (U601/U600)

On the CB3067 board there are two SO-DIMM260 memory slots for DDR4-2666 RAM. For technical and mechanical reasons, it is possible that certain memory modules cannot be used. Information regarding the recommended memory modules can be obtained from your distributor.

With four slots, a memory extension up to 64 GB is possible with currently available modules. When populating both memory slots, make sure that you use identical memory modules.

All timing parameters for the different makes and versions are automatically set by the BIOS.

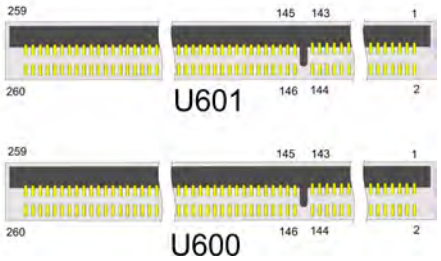


Fig. 13: CB3067-SO-DIMM260 (U601/U600)

Pin assignment SO-DIMM260					
Description	**Name**	**Pin**		**Name**	**Description**
Ground	GND	1	2	GND	Ground
Data line 5	DQ5	3	4	DQ4	Data line 4
Ground	GND	5	6	GND	Ground
Data line 1	DQ1	7	8	DQ0	Data line 0
Ground	GND	9	10	GND	Ground
Data strobe 0 -	DQS0#	11	12	NC	Not connected
Data strobe 0 +	DQS0	13	14	GND	Ground
Ground	GND	15	16	DQ6	Data line 6
Data line 7	DQ7	17	18	GND	Ground
Ground	GND	19	20	DQ2	Data line 2
Data line 3	DQ3	21	22	GND	Ground
Ground	GND	23	24	DQ12	Data line 12
Data line 13	DQ13	25	26	GND	Ground
Ground	GND	27	28	DQ8	Data line 8
Data line 9	DQ9	29	30	GND	Ground
Ground	GND	31	32	DQS1#	Data strobe 1 -
Data Mask 1	DQM1	33	34	DQS1	Data strobe 1 +
Ground	GND	35	36	GND	Ground
Data line 15	DQ15	37	38	DQ14	Data line 14
Ground	GND	39	40	GND	Ground
Data line 10	DQ10	41	42	DQ11	Data line 11
Ground	GND	43	44	GND	Ground
Data line 21	DQ21	45	46	DQ20	Data line 20
Ground	GND	47	48	GND	Ground
Data line 17	DQ17	49	50	DQ16	Data line 16
Ground	GND	51	52	GND	Ground
Data strobe 2 -	DQS2#	53	54	DQM2	Data Mask 2
Data strobe 2 +	DQS2	55	56	GND	Ground
Ground	GND	57	58	DQ22	Data line 22
Data line 23	DQ23	59	60	GND	Ground
Ground	GND	61	62	DQ18	Data line 18
Data line 19	DQ19	63	64	GND	Ground
Ground	GND	65	66	DQ28	Data line 28
Data line 29	DQ29	67	68	GND	Ground
Ground	GND	69	70	DQ24	Data line 24
Data line 25	DQ25	71	72	GND	Ground
Ground	GND	73	74	DQS3#	Data strobe 3 -
Data Mask 3	DQM3	75	76	DQS3	Data strobe 3 +
Ground	GND	77	78	GND	Ground
Data line 30	DQ30	79	80	DQ31	Data line 31
Ground	GND	81	82	GND	Ground
Data line 26	DQ26	83	84	DQ27	Data line 27
Ground	GND	85	86	GND	Ground
Not connected	CB5/NC	87	88	CB4/NC	Not connected
Ground	GND	89	90	GND	Ground
Not connected	CB1/NC	91	92	CB0/NC	Not connected
Ground	GND	93	94	GND	Ground

Pin assignment SO-DIMM260					
Description	**Name**	**Pin**		**Name**	**Description**
Data strobe 8 -	DQS8#	95	96	DQM8	Data Mask 8
Data strobe 8 +	DQS8	97	98	GND	Ground
Ground	GND	99	100	CB6/NC	Not connected
Not connected	CB2/NC	101	102	GND	Ground
Ground	GND	103	104	CB7/NC	Not connected
Not connected	CB3/NC	105	106	GND	Ground
Ground	GND	107	108	RESET_n	Reset
Clock Enable 0	CKE0	109	110	CKE1	Clock Enable 1
1.2 V supply voltage	VCC	111	112	VCC	1.2 V supply voltage
Bank Group Input 1	BG1	113	114	ACT_n	Activation Command Input
Bank Group Input 0	BG0	115	116	ALERT_n	Alert
1.2 V supply voltage	VCC	117	118	VCC	1.2 V supply voltage
Address line 12	O12	119	120	A11	Address line 11
Address line 9	A9	121	122	A7	Address line 7
1.2 V supply voltage	VCC	123	124	VCC	1.2 V supply voltage
Address line 8	A8	125	126	A5	Address line 5
Address line 6	A6	127	128	A4	Address line 4
1.2 V supply voltage	VCC	129	130	VCC	1.2 V supply voltage
Address line 3	A3	131	132	A2	Address line 2
Address line 1	A1	133	134	EVENT_n	Event
1.2 V supply voltage	VCC	135	136	VCC	1.2 V supply voltage
Clock Signal 0 +	CK0	137	138	CK1	Clock 1+
Clock Signal 0 -	CK0#	139	140	CK1#	Clock 1 -
1.2 V supply voltage	VCC	141	142	VCC	1.2 V supply voltage
Even parity check	PAR	143	144	A0	Address line 0
SDRAM Bank 2	BA1	145	146	A10/AP	Address line10/ auto precharge
1.2 V supply voltage	VCC	147	148	VCC	1.2 V supply voltage
Chip Select 0	CS0_n	149	150	BA0	Bank Address 0
Address line 14/Write Enable	A14/WE_n	151	152	A16/RAS_n	Address line 16/ Row Address Strobe
1.2 V supply voltage	VCC	153	154	VCC	1.2 V supply voltage
On Die Termination 0	ODT0	155	156	A15/CAS_n	Address line 15/ Column Address Strobe
Chip Select 1	CS1_n	157	158	O13	Address line 13
1.2 V supply voltage	VCC	159	160	VCC	1.2 V supply voltage
On Die Termination 1	ODT1	161	162	S2/NC	Not connected
1.2 V supply voltage	VCC	163	164	VREFCA	Reference voltage
Not connected	S3/NC	165	166	SA2	SPD Address 2
Ground	GND	167	168	GND	Ground
Data line 37	DQ37	169	170	DQ36	Data line 36
Ground	GND	171	172	GND	Ground
Data line 33	DQ33	173	174	DQ32	Data line 32
Ground	GND	175	176	GND	Ground
Data strobe 4 -	DQS4#	177	178	DQM4	Data Mask 4
Data strobe 4 +	DQS4	179	180	GND	Ground
Ground	GND	181	182	DQ39	Data line 39

Pin assignment SO-DIMM260					
Description	**Name**	**Pin**		**Name**	**Description**
Data line 38	DQ38	183	184	GND	Ground
Ground	GND	185	186	DQ35	Data line 35
Data line 34	DQ34	187	188	GND	Ground
Ground	GND	189	190	DQ45	Data line 45
Data line 44	DQ44	191	192	GND	Ground
Ground	GND	193	194	DQ41	Data line 41
Data line 40	DQ40	195	196	GND	Ground
Ground	GND	197	198	DQS5#	Data strobe 5 -
Not connected	NC	199	200	DQS5	Data strobe 5 +
Ground	GND	201	202	GND	Ground
Data line 46	DQ46	203	204	DQ47	Data line 47
Ground	GND	205	206	GND	Ground
Data line 42	DQ42	207	208	DQ43	Data line 43
Ground	GND	209	210	GND	Ground
Data line 52	DQ52	211	212	DQ53	Data line 53
Ground	GND	213	214	GND	Ground
Data line 49	DQ49	215	216	DQ48	Data line 48
Ground	GND	217	218	GND	Ground
Data strobe 6 -	DQS6#	219	220	DQM6	Data Mask 6
Data strobe 6 +	DQS6	221	222	GND	Ground
Ground	GND	223	224	DQ54	Data line 54
Data line 55	DQ55	225	226	GND	Ground
Ground	GND	227	228	DQ50	Data line 50
Data line 51	DQ51	229	230	GND	Ground
Ground	GND	231	232	DQ60	Data line 60
Data line 61	DQ61	233	234	GND	Ground
Ground	GND	235	236	DQ57	Data line 57
Data line 56	DQ56	237	238	GND	Ground
Ground	GND	239	240	DQS7#	Data strobe 7 -
Data Mask 7	DQM7	241	242	DQS7	Data strobe 7 +
Ground	GND	243	244	GND	Ground
Data line 62	DQ62	245	246	DQ63	Data line 63
Ground	GND	247	248	GND	Ground
Data line 58	DQ58	249	250	DQ59	Data line 59
Ground	GND	251	252	GND	Ground
SMBus Clock	SCL	253	254	SDA	SMBus Data
I²C power for SPD EEProm	VCCSPD	255	256	SA0	SPD Address 0
DRAM Activating Power	VPP	257	258	M_VTT	Termination voltage
DRAM Activating Power	VPP	259	260	SA1	SPD Address 1

6.13 USB 2.0 internal (P1202/P1204)

USB channels 9 - 14 are provided via two connectors.

Channels 9 to 12 are fed out via a 2x8-pin connector, channels 13 and 14 via a 2x4-pin connector.

The USB channels support the USB specification 2.0. All necessary settings for USB can be made by the BIOS. Note that the "USB mouse and keyboard" function in the BIOS setup is only required if the operating system does not offer USB support. This function should not be selected for settings in the setup and for booting Windows with a USB mouse and keyboard connected, because this would lead to considerable performance limitations.

The individual USB interfaces can supply a current of up to 500 mA and are electronically protected.

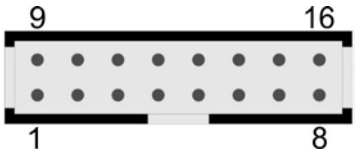


Fig. 14: CB3067 USB 2.0 (P1204)

Pin assignment 2x8-pin connector USB 9 - 12					
Description	**Name**	**Pin**		**Name**	**Description**
5 V for USB9	VCC	1	9	VCC	5 V for USB10
Minus data channel USB9	USB9-	2	10	USB10-	Minus data channel US10
Plus data channel USB9	USB9+	3	11	USB10+	Plus data channel USB10
Ground	GND	4	12	GND	Ground
Ground	GND	5	13	GND	Ground
Plus data channel USB12	USB12+	6	14	USB11+	Plus data channel USB11
Minus data channel USB12	USB12-	7	15	USB11-	Minus data channel USB11
5 V for USB12	VCC	8	16	VCC	5 V for USB11

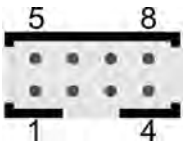


Fig. 15: CB3067 USB 2.0 (P1202)

Pin assignment 2x4-pin connector USB 13/14					
Description	**Name**	**Pin**		**Name**	**Description**
5 V for USB13	VCC	1	5	VCC	5 V for USB14
Minus data channel USB13	USB13-	2	6	USB14-	Minus data channel US14
Plus data channel USB13	USB13+	3	7	USB14+	Plus data channel USB14
Ground	GND	4	8	GND	Ground

6.14 System connector (P1102)

A 2x12-pin connector is used for the connection of signals that are typical of the system. Power button, reset, speaker, LEDs for hard disk and for Suspend mode are connected here along with three further status LEDs that are controlled via GPIOs. Of these three LEDs, LED1 and LED2 are already equipped with series resistors. The pin assignment is designed so that associated pins are located opposite or near to each other.

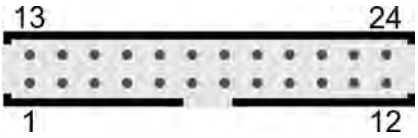


Fig. 16: CB3067 system connector (P1102)

Pin assignment system connector					
Description	**Name**	**Pin**		**Name**	**Description**
Ground	GND	1	14	3.3 V	3.3 V supply voltage
Reset to ground	RSTBTTN#	2	14	PWRBTN#	On/Suspend button
LED Suspend / ACPI	S-LED	3	15	S3.3V	Standby supply 3.3 V
LED hard disk	SATALED	4	16	GPIOLED3	LED GPIO device 3
LED GPIO device 1	GPIOLED1	5	17	BATT	RTC Battery
LED GPIO device 2	GPIOLED2	6	18	SMBALERT#	SMB Alert
SMB Clock	SMBCLKEX	7	19	SMBDATEXT	SMB Data
Speaker	SPEAKER	8	20	S VCC	Standby supply 5 V
Reserved	NC	9	21	NC	Reserved
Ground	GND	10	22	VCC	5 V supply voltage
Ground	GND	11	23	VCC	5 V supply voltage
Ground	GND	12	24	VCC	5 V supply voltage

6.15 PCI-Express connector (P1101)

The CB3067 is equipped with a vendor-specific 2x40-pin connector, via which PCI-Express devices can be connected. Either up to four PCIe1x devices or precisely one PCIe x4 device can be connected. Adapter cards with standard PCIe slots as well as with PCIe Mini-Card connectors are available as accessories. Please contact your distributor for this.

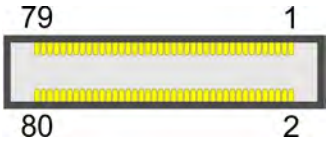


Fig. 17: CB3067 PCIE (P1101)

Pin assignment PCI-Express connector					
Description	**Name**	**Pin**		**Name**	**Description**
3.3 V supply voltage	3.3V	1	2	12V	12 V supply voltage
Standby supply 3.3 V	S3.3V	3	4	SMCLK1	SMB Clock Slot 1
PCIe Reset 1 -	PERST1#	5	6	SMDAT1	SMB Data Slot 1
Link Reactivation 1 -	WAKE1#	7	8	GND	Ground
Ground	GND	9	10	REFCLK1	PCIe Clock 1 +
Transmit Lane 1 +	PET1	11	12	REFCLK1#	PCIe Clock 1 -
Transmit Lane 1 -	PET1#	13	14	GND	Ground
Ground	GND	15	16	PER1	Receive Lane 1 +
Clock Enable 1 -	PRSNT1#	17	18	PER1#	Receive Lane 1 -
Ground	GND	19	20	GND	Ground
3.3 V supply voltage	3.3V	21	22	12V	12 V supply voltage
Standby supply 3.3 V	S3.3V	23	24	SMCLK2	SMB Clock Slot 2
PCIe Reset 2 -	PERST2#	25	26	SMDAT2	SMB Data Slot 2
Link Reactivation 2 -	WAKE2#	27	28	GND	Ground
Ground	GND	29	30	REFCLK2	PCIe Clock 2 +
Transmit Lane 2 +	PET2	31	32	REFCLK2#	PCIe Clock 2 -
Transmit Lane 2 -	PET2#	33	34	GND	Ground
Ground	GND	35	36	PER2	Receive Lane 2 +
Clock Enable 2 -	PRSNT2#	37	38	PER2#	Receive Lane 2 -
Ground	GND	39	40	GND	Ground
3.3 V supply voltage	3.3V	41	42	12V	12 V supply voltage
Standby supply 3.3 V	S3.3V	43	44	SMCLK3	SMB Clock Slot 3
PCIe Reset 3 -	PERST3#	45	46	SMDAT3	SMB Data Slot 3
Link Reactivation 3 -	WAKE3#	47	48	GND	Ground
Ground	GND	49	50	REFCLK3	PCIe Clock 3 +
Transmit Lane 3 +	PET3	51	52	REFCLK3#	PCIe Clock 3 -
Transmit Lane 3 -	PET3#	53	54	GND	Ground
Ground	GND	55	56	PER3	Receive Lane 3 +
Clock Enable 3 -	PRSNT3#	57	58	PER3#	Receive Lane 3 -
Ground	GND	59	60	GND	Ground
3.3 V supply voltage	3.3V	61	62	12V	12 V supply voltage
Standby supply 3.3 V	S3.3V	63	64	SMCLK4	SMB Clock Slot 4
PCIe Reset 4 -	PERST4#	65	66	SMDAT4	SMB Data Slot 4
Link Reactivation 4 -	WAKE4#	67	68	GND	Ground
Ground	GND	69	70	REFCLK4	PCIe Clock 4 +
Transmit Lane 4 +	PET4	71	72	REFCLK4#	PCIe Clock 4 -
Transmit Lane 4 -	PET4#	73	74	GND	Ground
Ground	GND	75	76	PER4	Receive Lane 4 +
Clock Enable 4 -	PRSNT4#	77	78	PER4#	Receive Lane 4 -
PCIe configuration x1/x4	PECONF x1/ x4	79	80	GND	Ground

7 Status LEDs

7.1 RGB LED

There is an RGB LED on the CB3067 with which status messages of the power controller are output by means of colors and flashing intervals.

Color	Interval	Meaning
None	Steadily lit	System in error state
White	Steadily lit	Power fail
Cyan	Steadily lit	Reserved
Magenta	Steadily lit	S UPS active (if present)
Blue	Steadily lit	Reserved
Yellow	Steadily lit	S5 state
Green	Steadily lit	S0 state
Red	Steadily lit	Reset/Start
Green/yellow	Flashing	Bootloader running without error
Red/yellow	Flashing	Bootloader is starting (start sequence is being run through)
Yellow	Flashing (6 s)	S4 state
Yellow	Flashing (3 s)	S3 state
Magenta	Flashing (0.5 s)	S UPS capacitance test (if S UPS present)
Red/magenta	Flashing	Checksum error during I^2C transmission in the boot loader

A steadily lit red LED can indicate a hardware error.

Adaptation of the status codes

It is possible to adapt the status codes (e.g. as TwinCAT LED). To do this, the system colors can be changed with the aid of an SMB command. This change remains in force until the next restart or reset. A change of the default colors is indicated by the additional flashing of the white LED.

8 BIOS settings

8.1 Using the setup

Within the individual setup pages the last saved settings can be restored at any time with F2 ("Previous Values"). Use F3 ("Optimized Defaults") to load the factory defaults. Use F2/F3 to load the complete set of settings and F4 to save them ("Save & Exit").

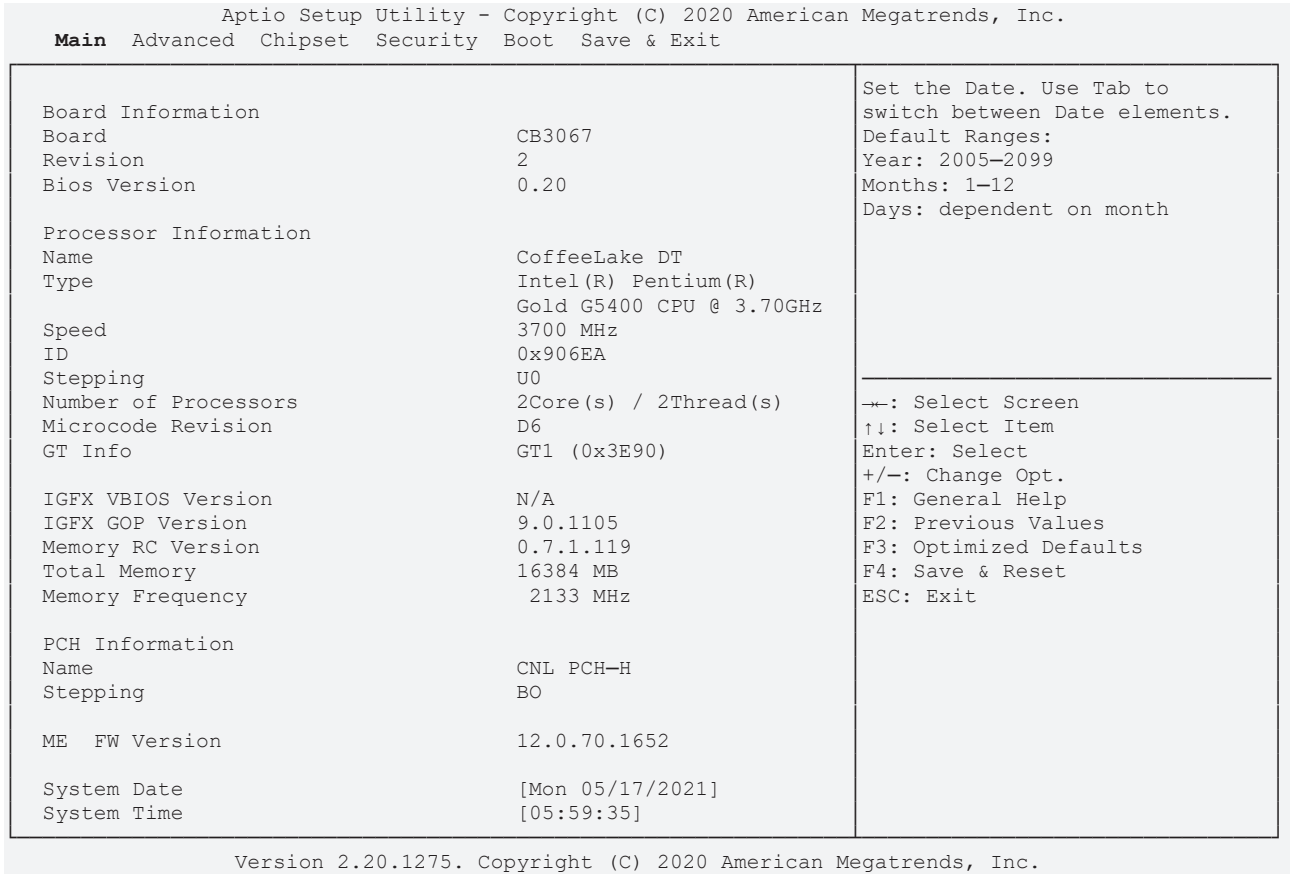
A "►" sign in front of the menu item indicates that a submenu is available. Use the arrow keys to navigate between menu items. Use the Enter key to select menu items and call submenus or selection dialogs.

For each setup option a help text is displayed at the top right, which in many cases contains useful information about the option and permitted values, etc.

Note on Setup Documentation

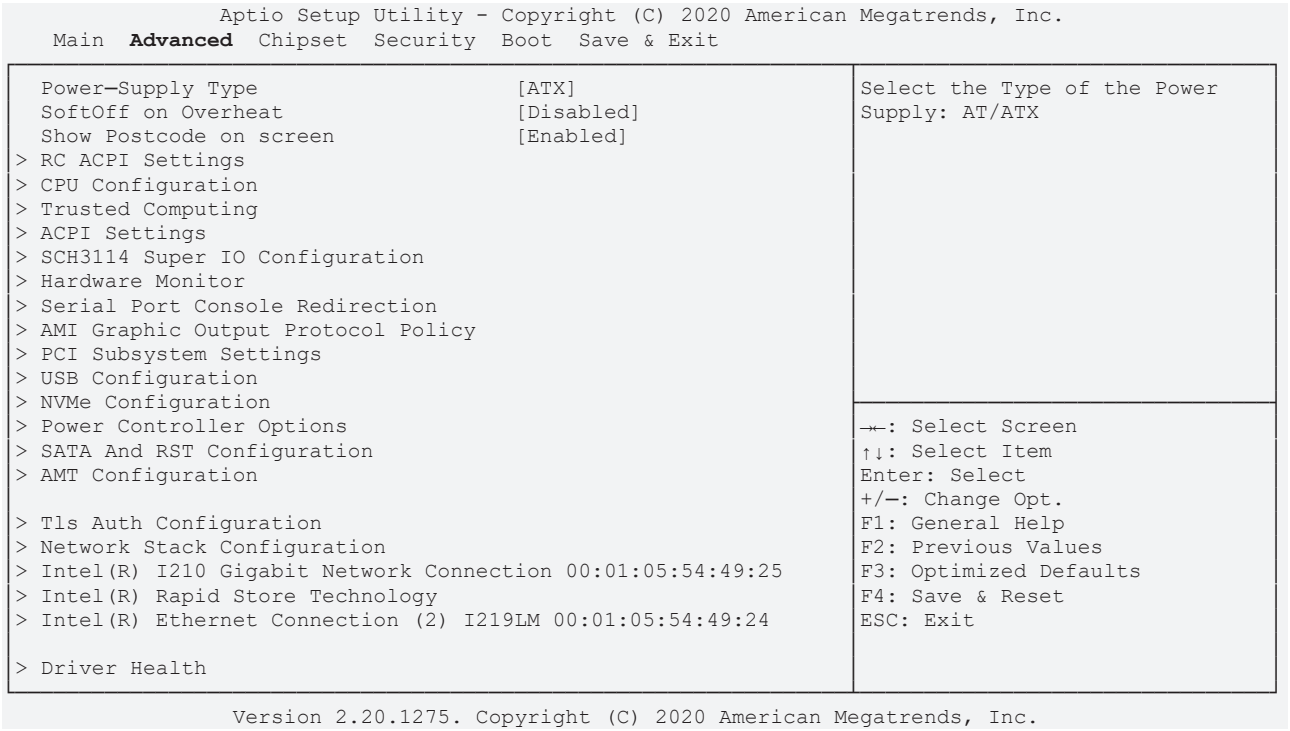
The BIOS is regularly updated so that the available setup options can change at any time without notice. This may result in differences between the options actually available and those described below. It should also be noted that the settings shown in the setup menus below are not necessarily the recommended or default settings. Which settings must be selected depends on the application scenario in which the board is operated.

8.2 Main



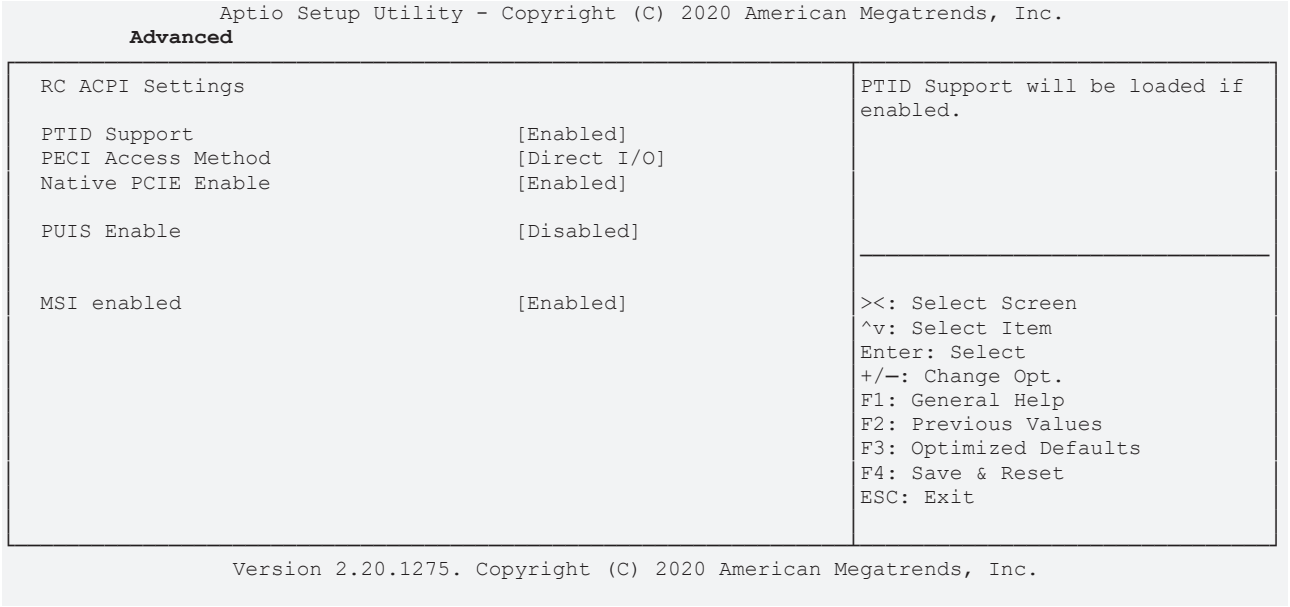
Bios entry	Option
Board information	
Board*	None
Revision	None
Bios version	None
Processor Information	
Name	None
Type	None
Speed	None
ID	None
Stepping	None
Number of Processors	None
Microcode Revision	None
GT info	None
IGFX VBIOS version	None
IGFX GOP version	None
Memory RC version	None
Total Memory	None
Memory Frequency	None
PCH information	
Name	None
Stepping	None
ME FW version	None
System Date	Here you can change the system date.
System Time	Here you can change the system time.

8.3 Advanced Menu



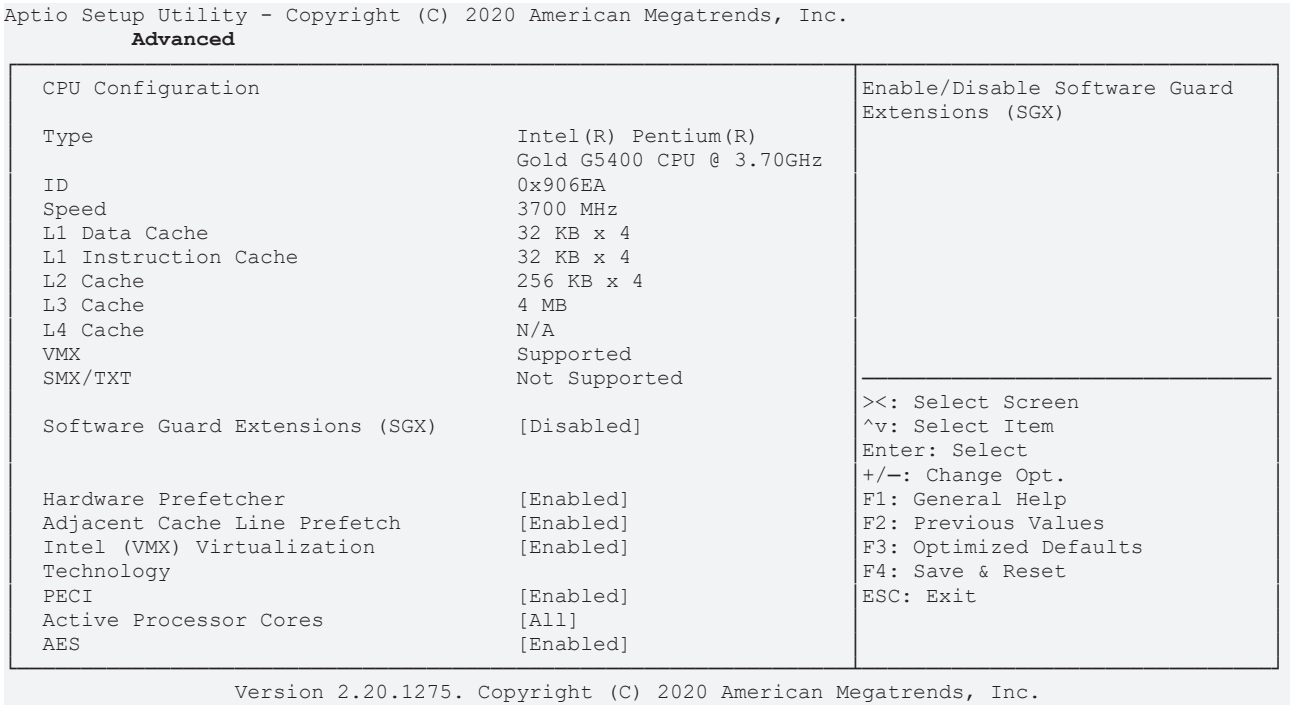
Bios entry	Option
Power-Supply Type	[ATX/AT]
SoftOff on overheat	Disabled / Enabled / Enabled (Emulate PwrBtn)
RC ACPI settings	Submenu see: RC ACPI settings [▶ 35]
CPU Configuration	Submenu see: CPU Configuration [▶ 36]
Trusted Computing	Submenu see: Trusted Computing [▶ 37]
ACPI Settings	Submenu see: ACPI Settings Enabled [▶ 37]
SCH3114 Super IO Configuration	Submenu see: SCH3114 Super IO Configuration [▶ 39]
Hardware Monitor	Submenu see: Hardware Monitor [▶ 44]
Serial Port Console Redirection	Submenu see: Serial Port Console Redirection [▶ 45]
AMI Graphic Output Protocol Policy	Submenu see: AMI Graphic Output Protocol Policy [▶ 50]
PCI Subsystem Settings	Submenu see: PCI Subsystem Settings [▶ 51]
USB Configuration	Submenu see: USB Configuration [▶ 53]
NVMe Configuration	Submenu see: NVMe Configuration [▶ 54]
Power Controller Options	Submenu see: Power Controller Options [▶ 55]
SATA And RST Configuration	Submenu see: SATA und RST Configuration [▶ 56]
AMT Configuration	Submenu see: AMT Configuration [▶ 58]
Tls Auth configuration	Submenu see: TLs Auth Configuration [▶ 62]
Network Stack Configuration	Submenu see: Network Stack Configuration [▶ 64]
Intel(R) I210 Gigabit Network Connection 00:01:05:52:C3:3D	Submenu see: NIC Configuration [▶ 68]
Intel® Rapid Store Technology	Submenu see: Intel Rapid Storage Technology [▶ 66]
Intel(R) Ethernet Connection (2) I219LM 00:01:05:52:C7:3C	Submenu see: NIC Configuration [▶ 70]
Driver Health	Submenu see: Driver Health [▶ 71]

8.3.1 RC ACPI settings



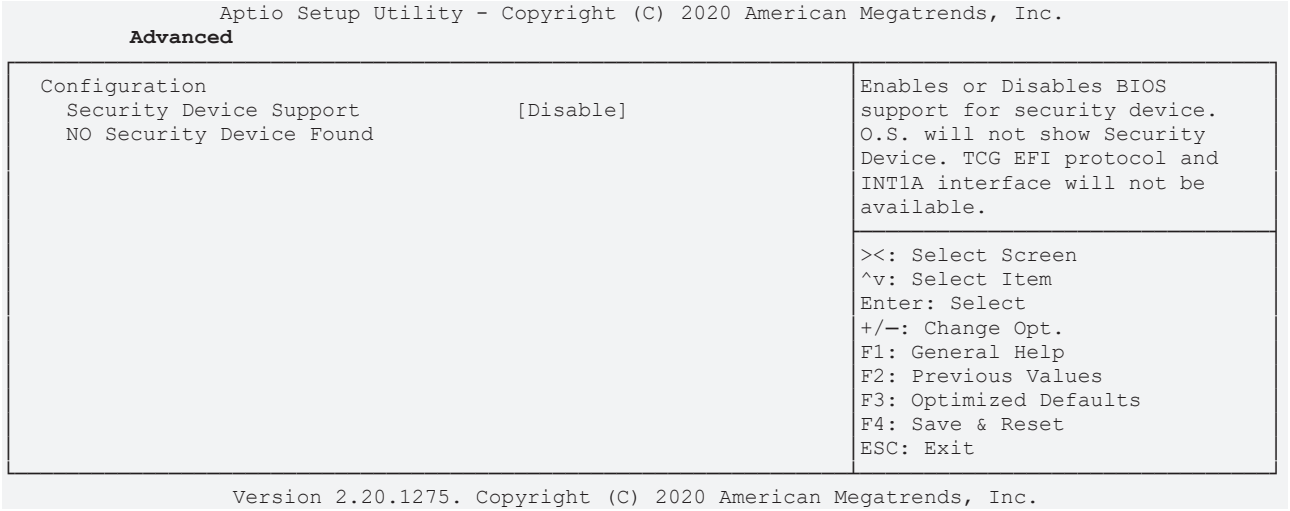
Bios entry	Options
RC ACPI settings	
PTID support	Enabled/Disabled
PECI access method	Direct I/O/ACPI
Native PCIE Enable	Enabled/Disabled
PUIS Enable	None
MSI enabled	Enabled/Disabled

8.3.2 CPU Configuration



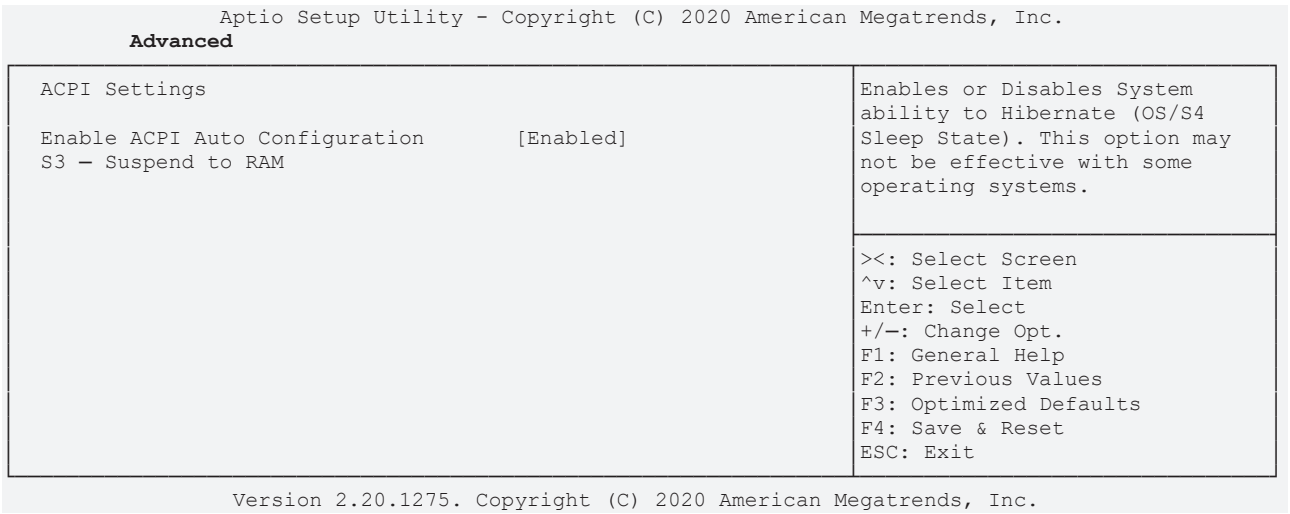
Bios entry	Options
CPU Configuration	
Type	None
ID	None
Speed	None
L1 Data Cache	None
L1 instruction cache	None
L2 Cache	None
L3 Cache	None
L4 cache	None
VMX	None
SMX/TXT	None
Software Guard Extensions (SGX)	Disabled/Enabled/Software Controlled
Hardware prefetcher	Enabled/Disabled
Adjacent Cache Line Prefetch	Enabled/Disabled
Intel (VMX) Virtualization Technology	Enabled/Disabled
PECI	Enabled/Disabled
Active Processor Cores	All/1/2/3
AES	Enabled/Disabled

8.3.3 Trusted Computing



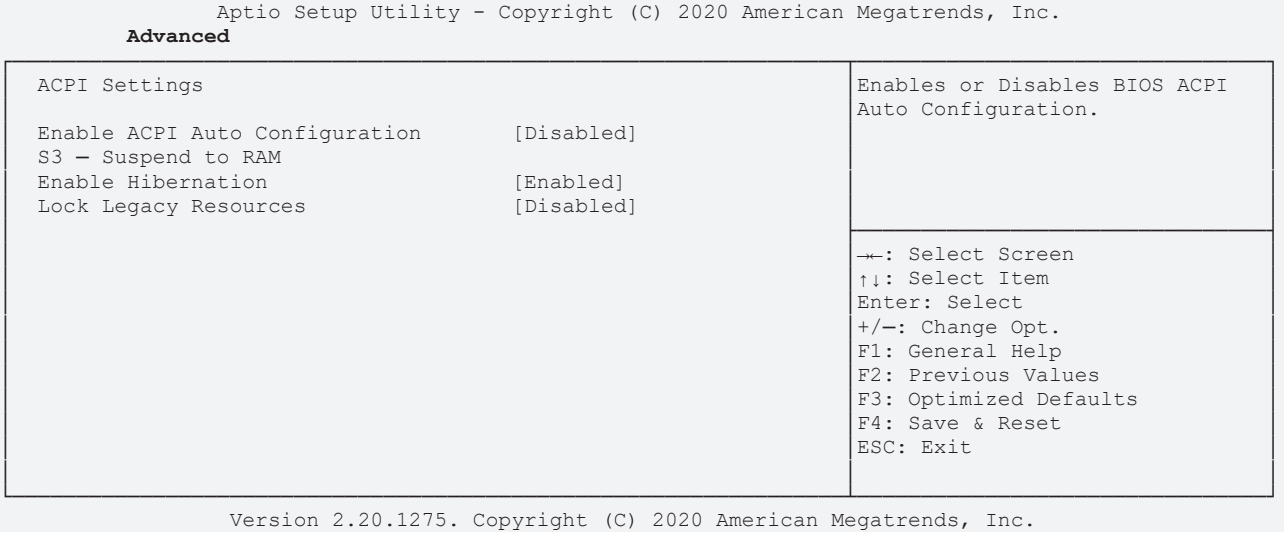
Bios entry	Options
Configuration	
Security device support	Disable/Enable
No security device found	None

8.3.4 ACPI Settings Enabled



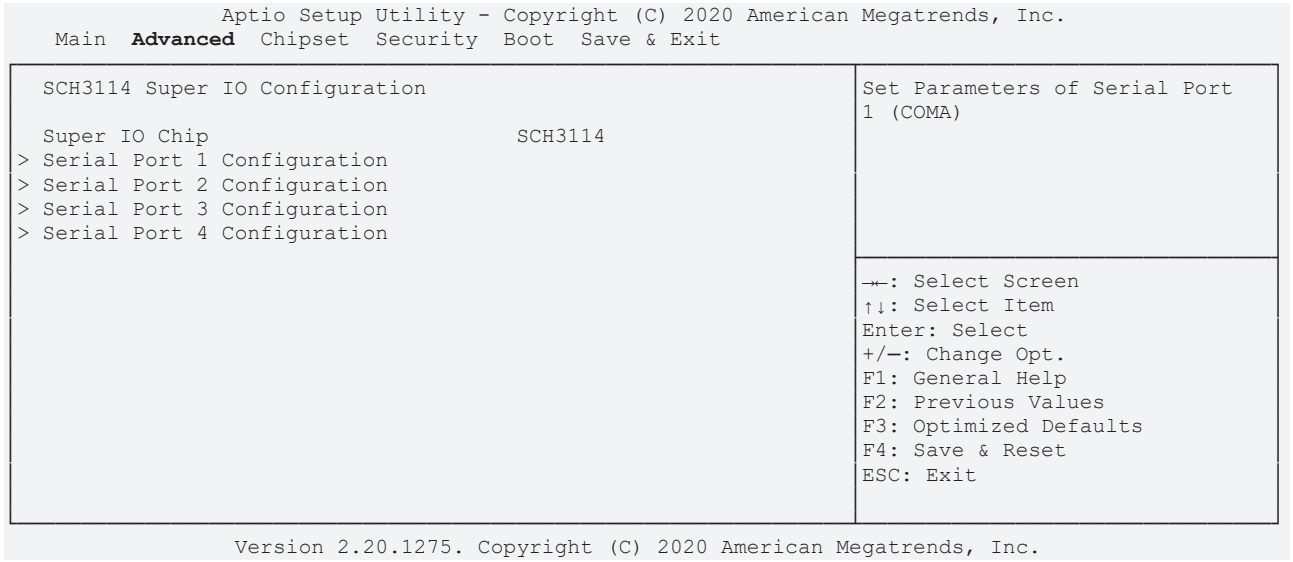
Bios entry	Options
ACPI Settings	
Enable ACPI Auto Configuration	Enabled/Disabled
S3 – Suspend to RAM	None

8.3.5 ACPI Settings Disabled



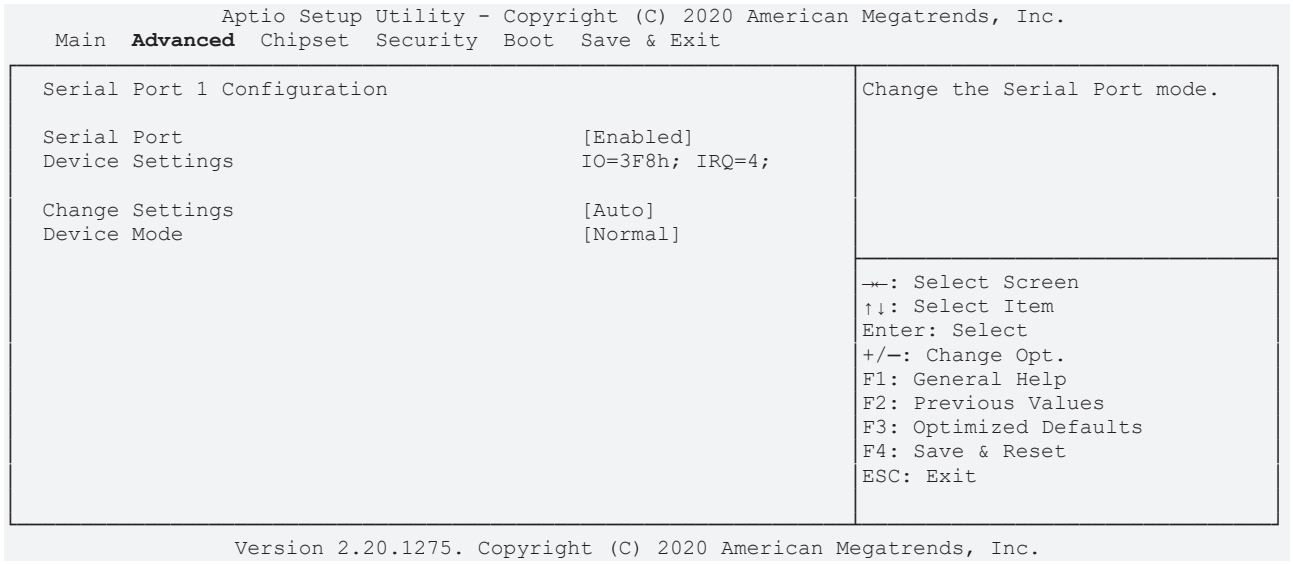
Bios entry	Options
ACPI Settings	
Enable ACPI Auto Configuration	Enabled/Disabled
S3 – Suspend to RAM	None
Enabale Hibernation	Disabled/Enabled
Lock Legacy Resources	Disabled/Enabled

8.3.6 SCH3114 Super IO Configuration



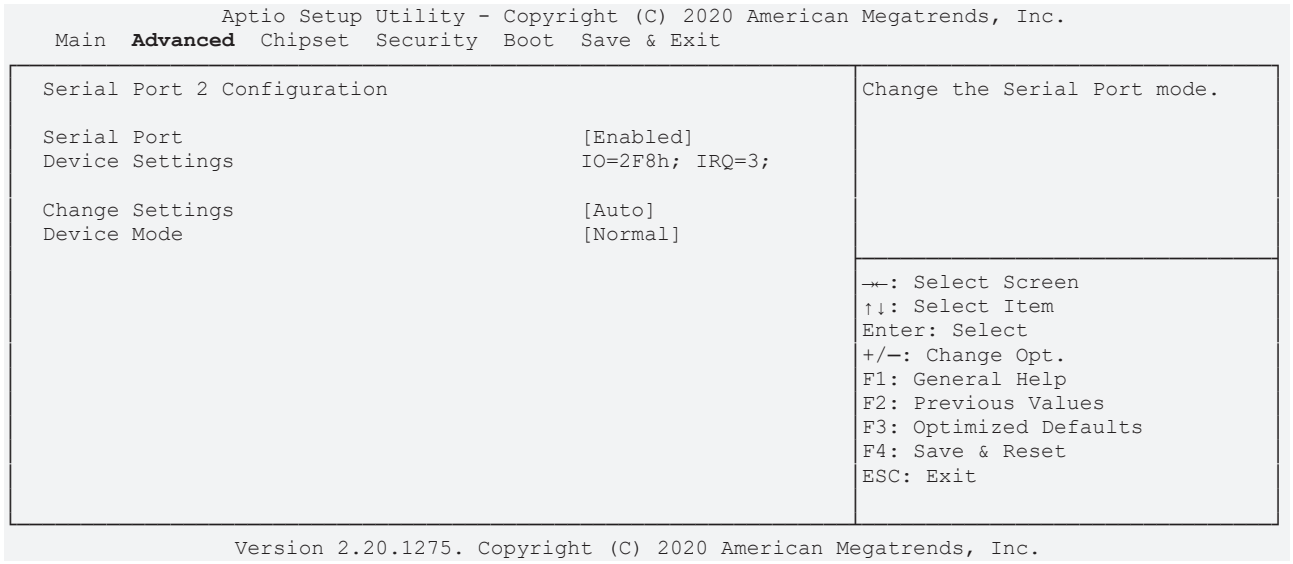
Bios entry	Options
SCH3114 Super IO Configuration	
Super IO Chip	
Serial Port 1 Configuration	Submenu see: Serial Port 1 Configuration [▶ 40]
Serial Port 2 Configuration	Submenu see: Serial Port 2 Configuration [▶ 41]
Serial Port 1 Configuration	Submenu see: Serial Port 3 Configuration [▶ 42]
Serial Port 2 Configuration	Submenu see: Serial Port 4 Configuration [▶ 43]

8.3.6.1 Serial Port 1 Configuration



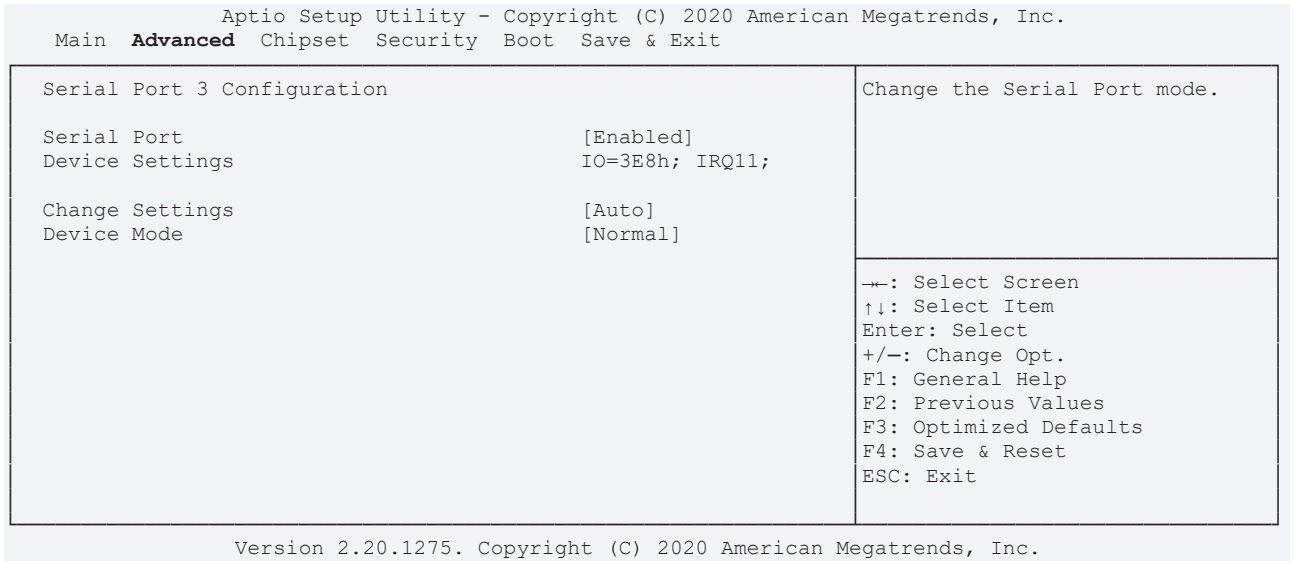
Bios entry	Options
Serial Port 1 Configuration	
Serial Port	Enabled/Disabled
Device Settings	None
Change Settings	Auto/IO=3F8h; IRQ=4;…IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12; and further
Device Mode	Normal/High Speed

8.3.6.2 Serial Port 2 Configuration



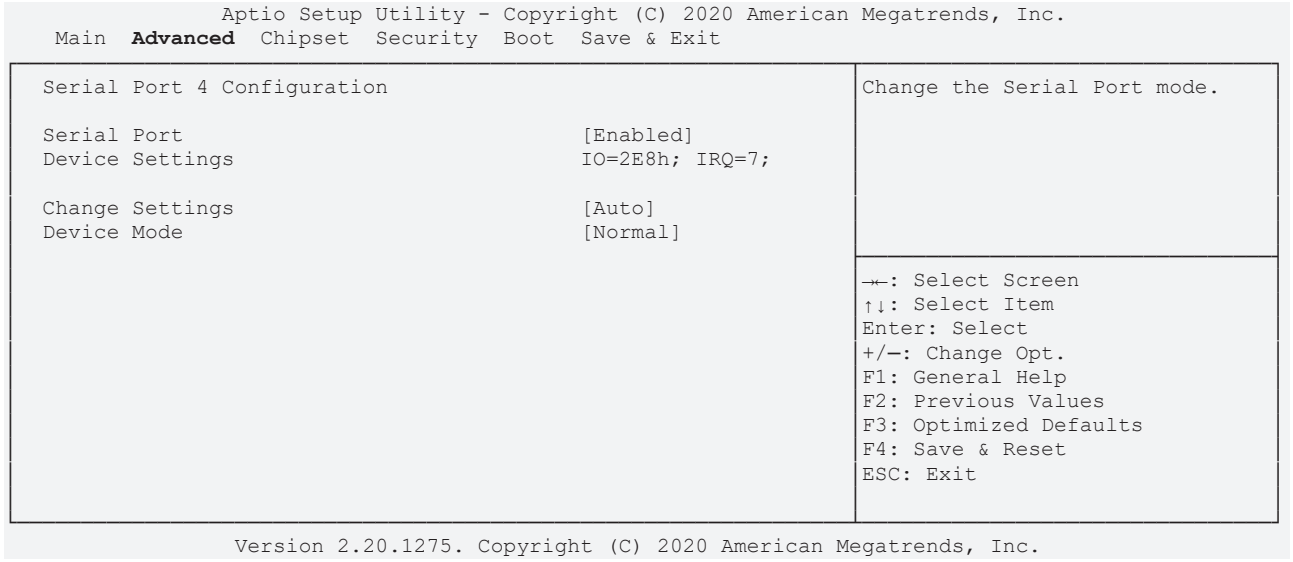
Bios entry	Options
Serial Port 2 Configuration	
Serial Port	Enabled/Disabled
Device Settings	None
Change Settings	Auto/IO=2F8h; IRQ=3;…IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12; and further
Device Mode	Normal/High Speed

8.3.6.3 Serial Port 3 Configuration



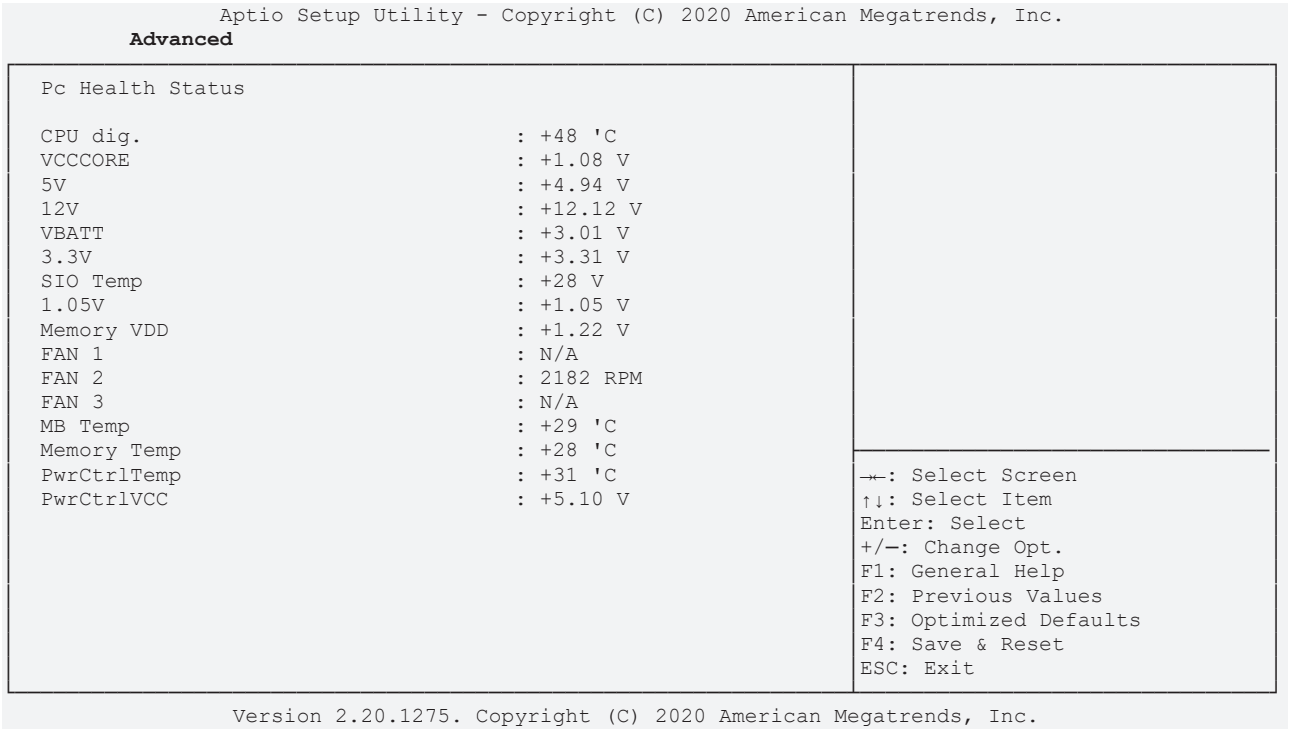
Bios entry	Options
Serial Port 3 Configuration	
Serial Port	Enabled/Disabled
Device Settings	None
Change Settings	Auto/IO=3E8h; IRQ=11;…IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12; and further
Device Mode	Normal/High Speed

8.3.6.4 Serial Port 4 Configuration



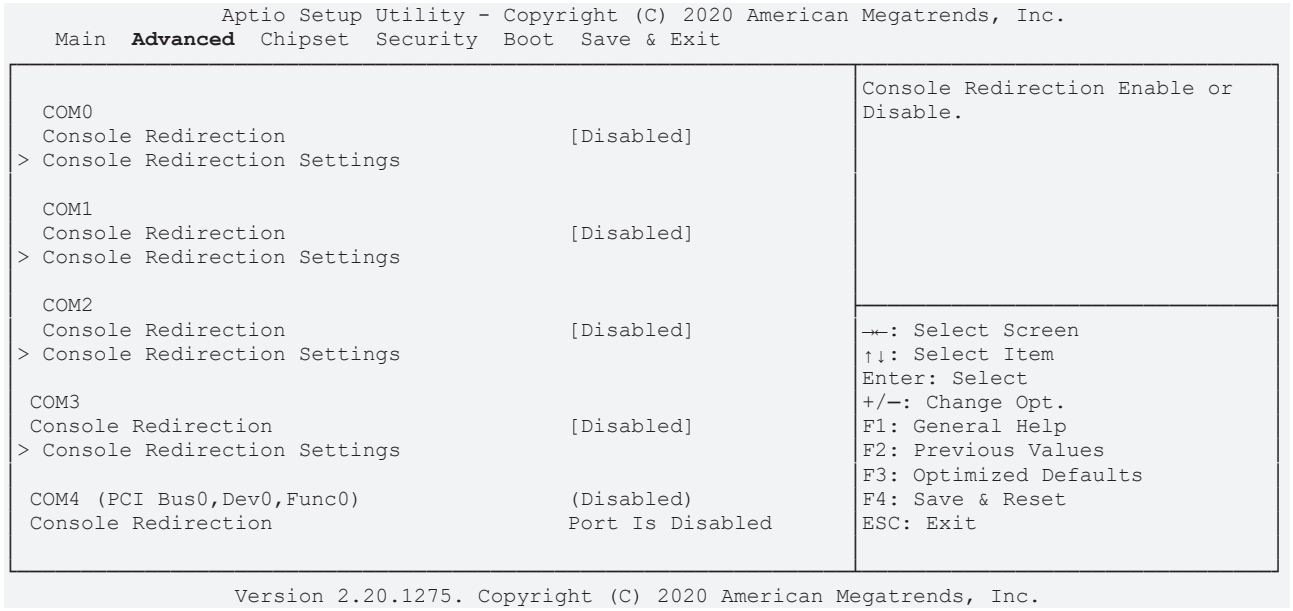
Bios entry	Options
Serial Port 4 Configuration	
Serial Port	Enabled/Disabled
Device Settings	None
Change Settings	Auto/IO=2E8h; IRQ=10;…IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12; and further
Device Mode	Normal/High Speed

8.3.7 Hardware Monitor



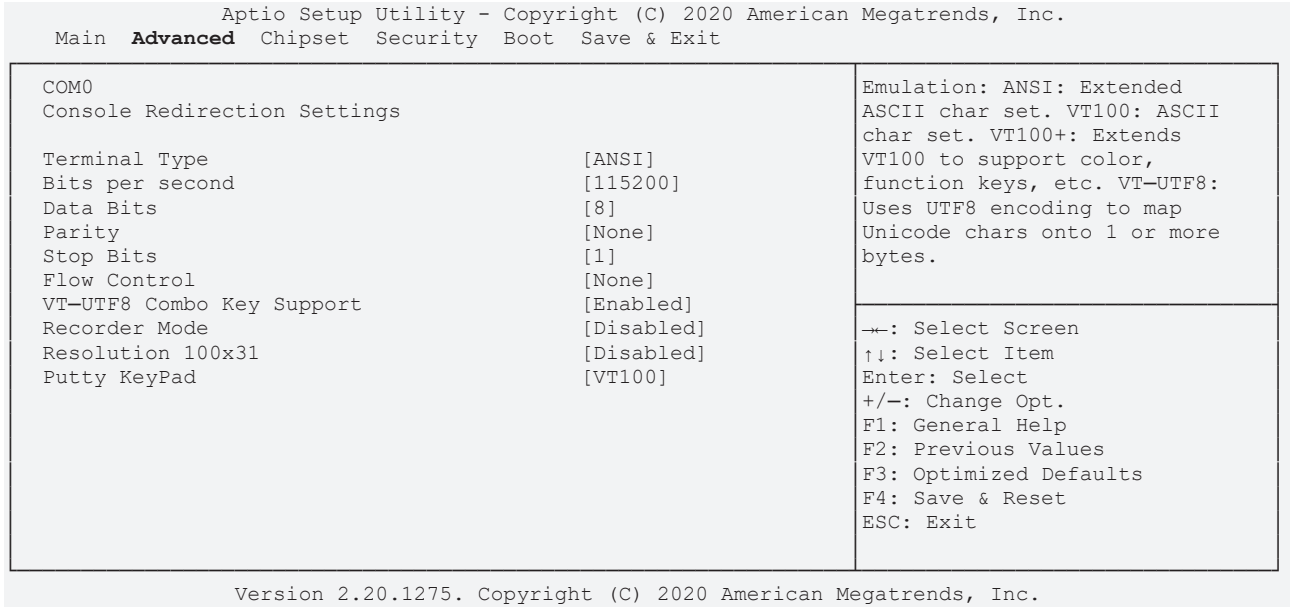
Bios entry	Options
PC Health Status	None

8.3.8 Serial Port Console Redirection



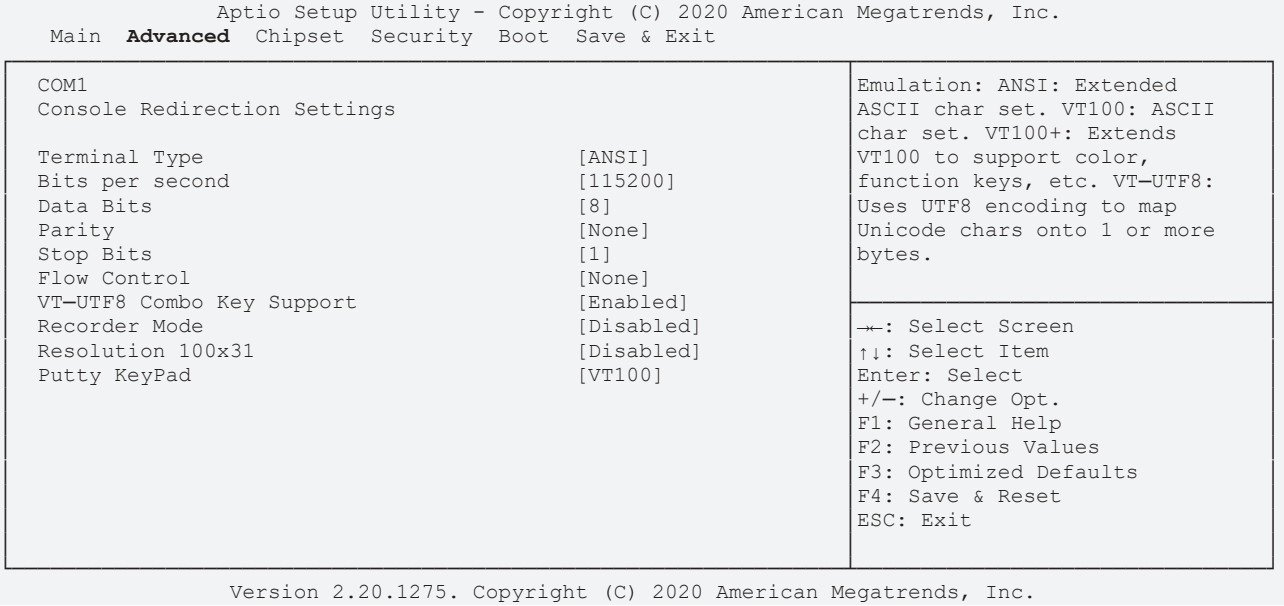
Bios entry	Options
COM0	
Console Redirection	Disabled/Enabled
Console Redirection Settings	Submenu see: COM0 Console Redirection Settings [▶ 46]
COM1	
Console Redirection	Disabled/Enabled
Console Redirection Settings	Submenu see: COM1 Console Redirection Settings [▶ 47]
COM2	
Console Redirection	Disabled/Enabled
Console Redirection Settings	Submenu see: COM2 Console Redirection Settings [▶ 48]
COM3	
Console Redirection	Disabled/Enabled
Console Redirection Settings	Submenu see: COM3 Console Redirection Settings [▶ 49]
COM4 (Pci Bus0, Dev0, Func0) (Disabled)	
Console Redirection	Port Is Disabled

8.3.8.1 COM0 Console Redirection Settings



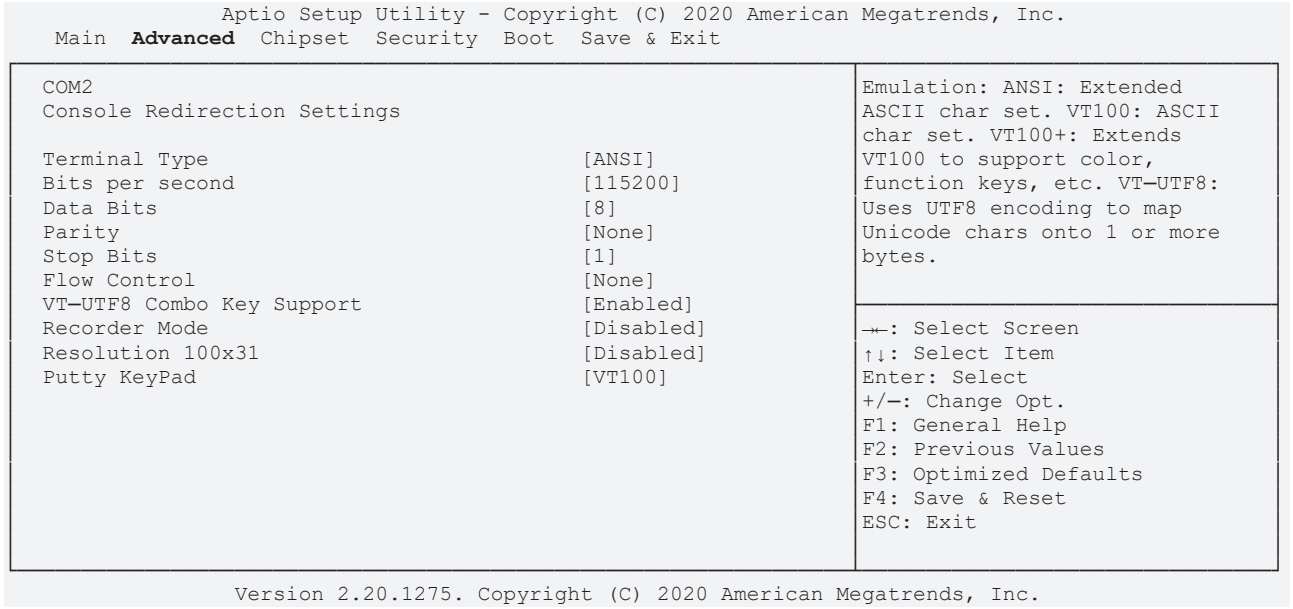
Bios entry	Options
COM0	
Console Redirection Settings	
Serial Port Terminal Type	VT100/VT100+/VT-UTF8/ANSI
Bits per second	9600/19200/38400/57600/115200
Data Bits	7/8
Parity	None/Even/Odd/Mark/Space
Stop Bits	1/2
Flow Control	None/Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enabled/Disabled
Recorder Mode	Disabled/Enabled
Resolution 100x31	Disabled/Enabled
Putty KeyPad	VT100/LINUX/XTERMR6/SCO/ESCN/VT400

8.3.8.2 COM1 Console Redirection Settings



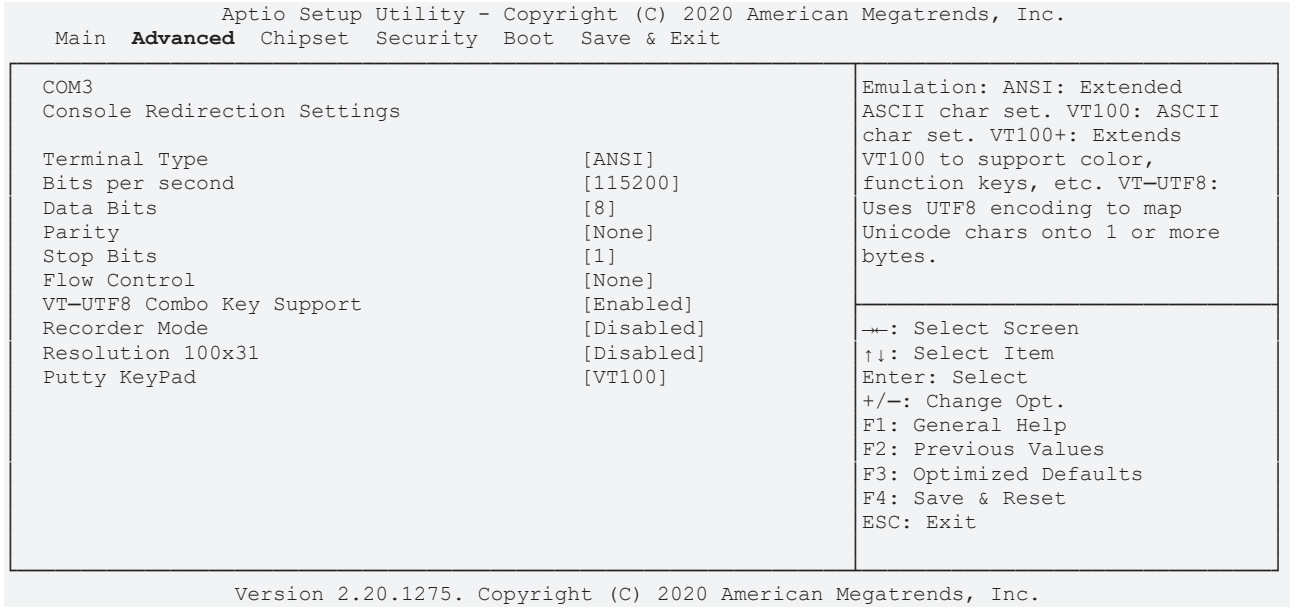
Bios entry	Options
COM1	
Console Redirection Settings	
Serial Port Terminal Type	VT100/VT100+/VT-UTF8/ANSI
Bits per second	9600/19200/38400/57600/115200
Data Bits	7/8
Parity	None/Even/Odd/Mark/Space
Stop Bits	1/2
Flow Control	None/Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enabled/Disabled
Recorder Mode	Disabled/Enabled
Resolution 100x31	Disabled/Enabled
Putty KeyPad	VT100/LINUX/XTERMR6/SCO/ESCN/VT400

8.3.8.3 COM2 Console Redirection Settings



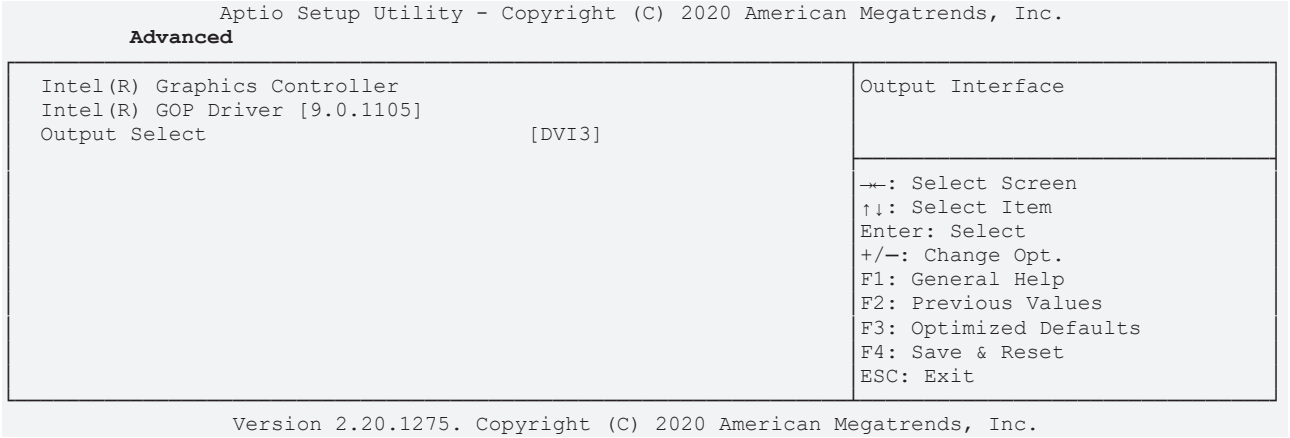
Bios entry	Options
COM2	
Console Redirection Settings	
Serial Port Terminal Type	VT100/VT100+/VT-UTF8/ANSI
Bits per second	9600/19200/38400/57600/115200
Data Bits	7/8
Parity	None/Even/Odd/Mark/Space
Stop Bits	1/2
Flow Control	None/Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enabled/Disabled
Recorder Mode	Disabled/Enabled
Resolution 100x31	Disabled/Enabled
Putty KeyPad	VT100/LINUX/XTERMR6/SCO/ESCN/VT400

8.3.8.4 COM3 Console Redirection Settings



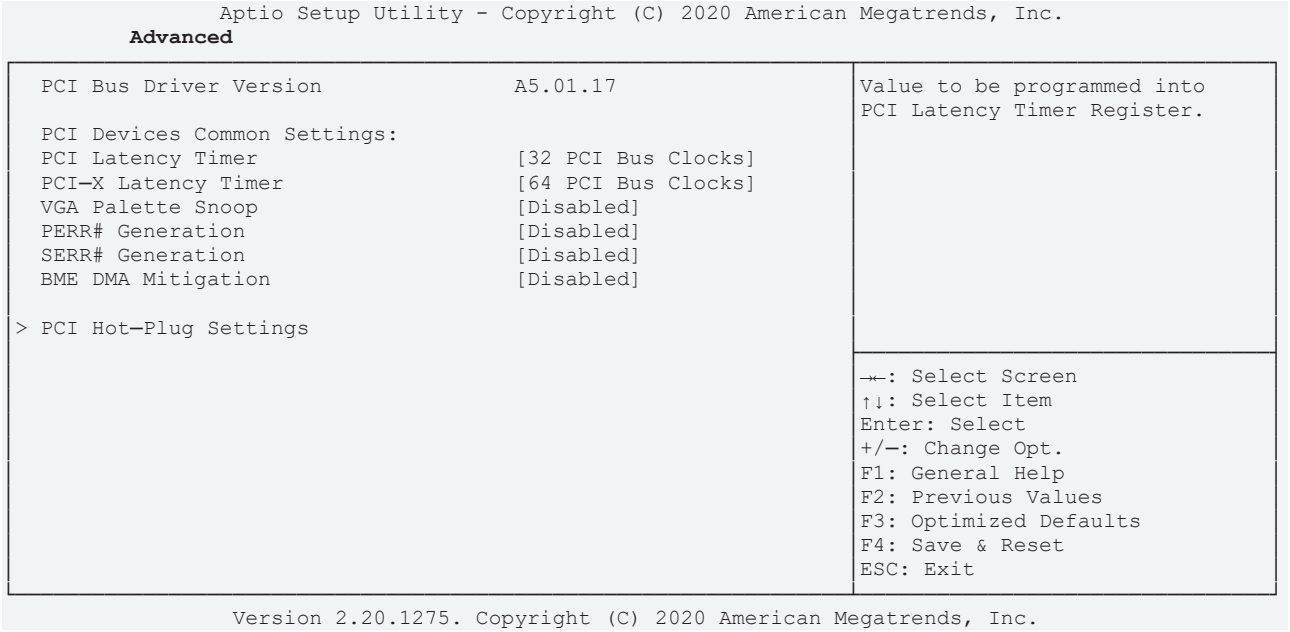
Bios entry	Options
COM3	
Console Redirection Settings	
Serial Port Terminal Type	VT100/VT100+/VT-UTF8/ANSI
Bits per second	9600/19200/38400/57600/115200
Data Bits	7/8
Parity	None/Even/Odd/Mark/Space
Stop Bits	1/2
Flow Control	None/Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enabled/Disabled
Recorder Mode	Disabled/Enabled
Resolution 100x31	Disabled/Enabled
Putty KeyPad	VT100/LINUX/XTERMR6/SCO/ESCN/VT400

8.3.9 AMI Graphic Output Protocol Policy



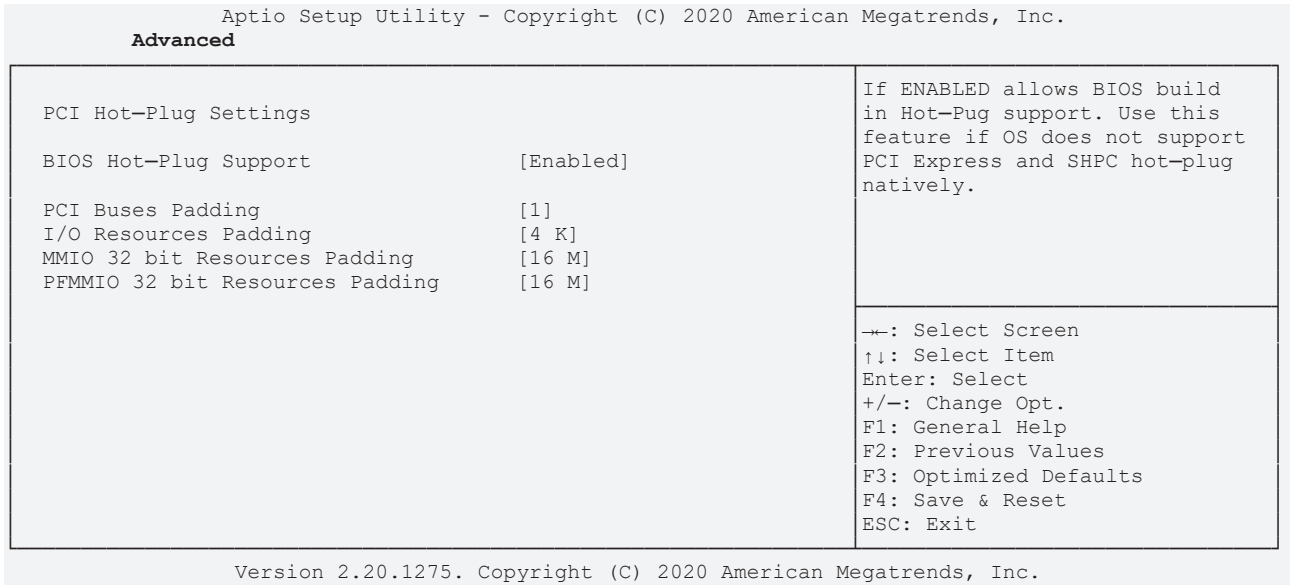
Bios entry	Options
Intel® Graphics Controller Intel® GOP Driver [9.0.1105]	
Output Select	None

8.3.10 PCI Subsystem Settings



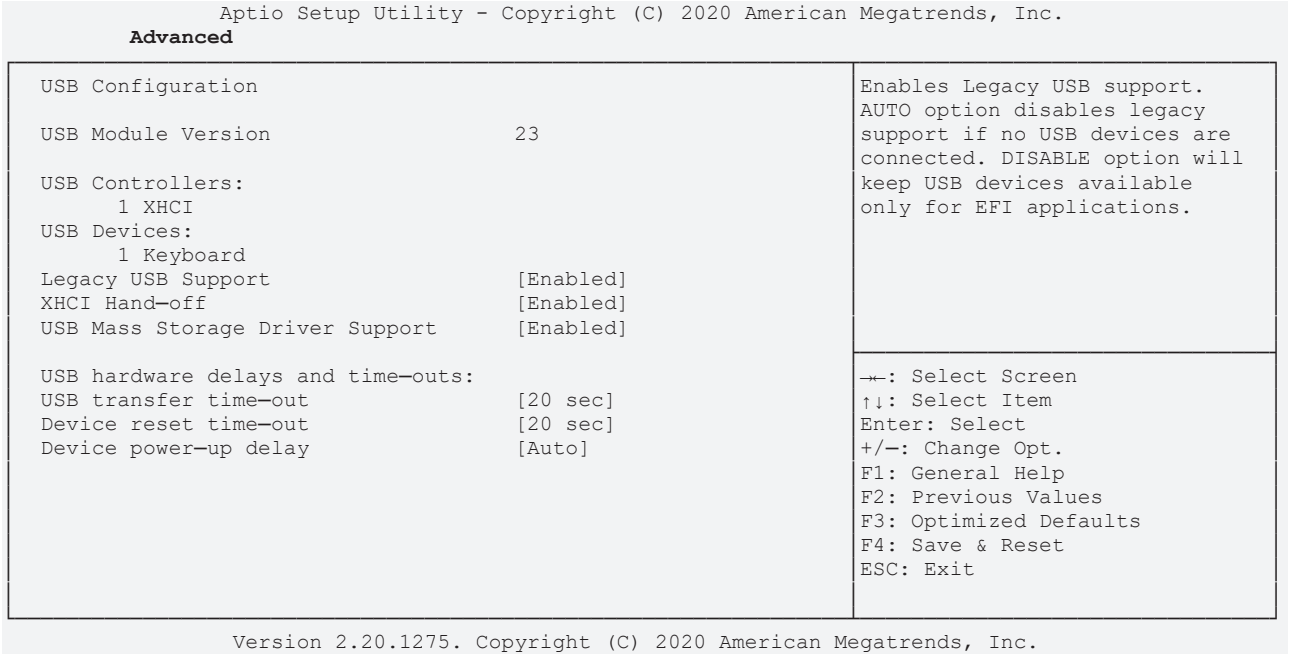
Bios entry	Options
PCI Bus Driver Version	None
PCI Device Common Settings:	
PCI Latency Timer	32/64/96/128/160/192/224/248/PCI Bus Clocks
PCI-X Latency Timer	32/64/96/128/160/192/224/248/PCI Bus Clocks
VGA Palette Snoop	Disabled/Enabled
PERR# Generation	Disabled/Enabled
SERR# Generation	Disabled/Enabled
Above 4G Decoding	Disabled/Enabled
PCI Hot-Plug Settings	Submenu see: PCI Hot-Plug Settings [▶ 52]

8.3.10.1 PCI Hot-Plug Settings



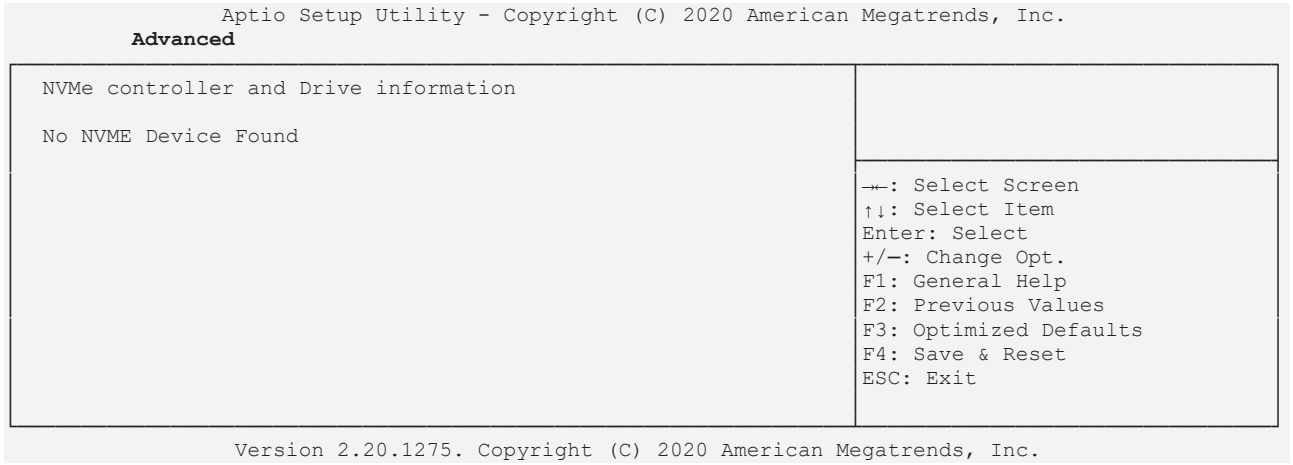
Bios entry	Options
PCI Hot-Plug Settings	
BIOS Hot-Plug Support	Enabled/Disabled
PCI Buses Padding	Disabled/1/2/3/4/5
I/O Resources Padding	Disabled/4 K/8 K/16 K/32 K
MMIO 32 bit Resources Padding	Disabled/1 M/2 M/4 M/8 M/16 M/32 M/64 M/128 M
PFMMIO 32 bit Resources Padding	Disabled/1 M/2 M/4 M/8 M/16 M/32 M/64 M/128 M

8.3.11 USB Configuration



Bios entry	Options
USB Configuration	
USB Module Version	None
USB Controllers: 1XHCI	None
USB Devices: 1 Keyboard	None
Legacy USB Support	Enabled/Disabled/Auto
XHCI Hand-off	Enabled/Disabled
USB Mass Storage Driver Support	Enabled/Disabled
USB hardware delays and time-outs:	
USB transfer time-out	1/5/10/20 sec
Device reset time-out	10/20/30/40 sec
Device power-up delay	Auto/Manual

8.3.12 NVMe Configuration

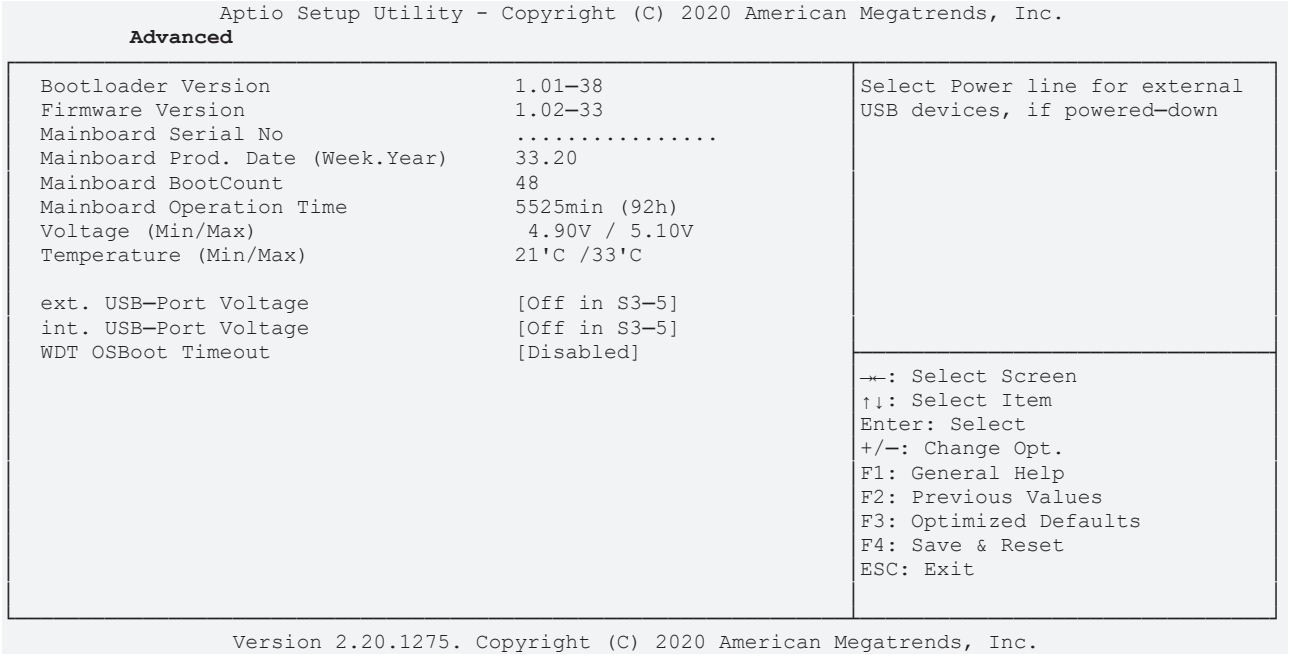


Bios entry	Options
NVMe controller and Drive Information	
No NVME Device Found	None

NOTE

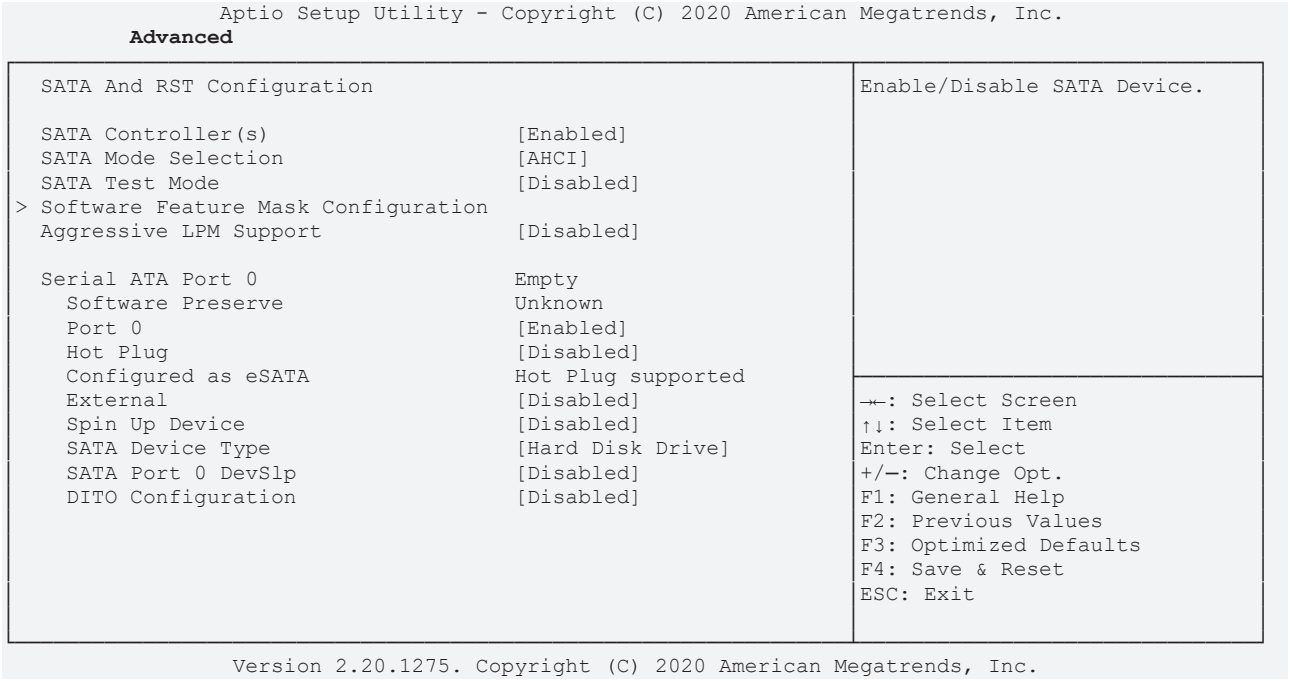
NVMe Raid 0/1 is not supported.

8.3.13 Power Controller Options



Bios entry	Options
Bootloader Version	None
Firmware Version	None
Mainboard Serial No	None
Mainboard Prod. Date (Week.Year)	None
Mainboard BootCount	None
Mainboard Operation Time	None
Voltage (Min/Max)	None
Temperature (Min/Max)	None
ext. USB-Port Voltage	Off in S3-5/by SCVV
int. USB-Port Voltage	Off in S3-5/by SCVV
WatchDogTimer mode	Normal Mode/Compatibility Mode
WDT OSBoot Timeout	Disabled/45, 60, 75,…225, 240, 255 seconds

8.3.14 SATA und RST Configuration



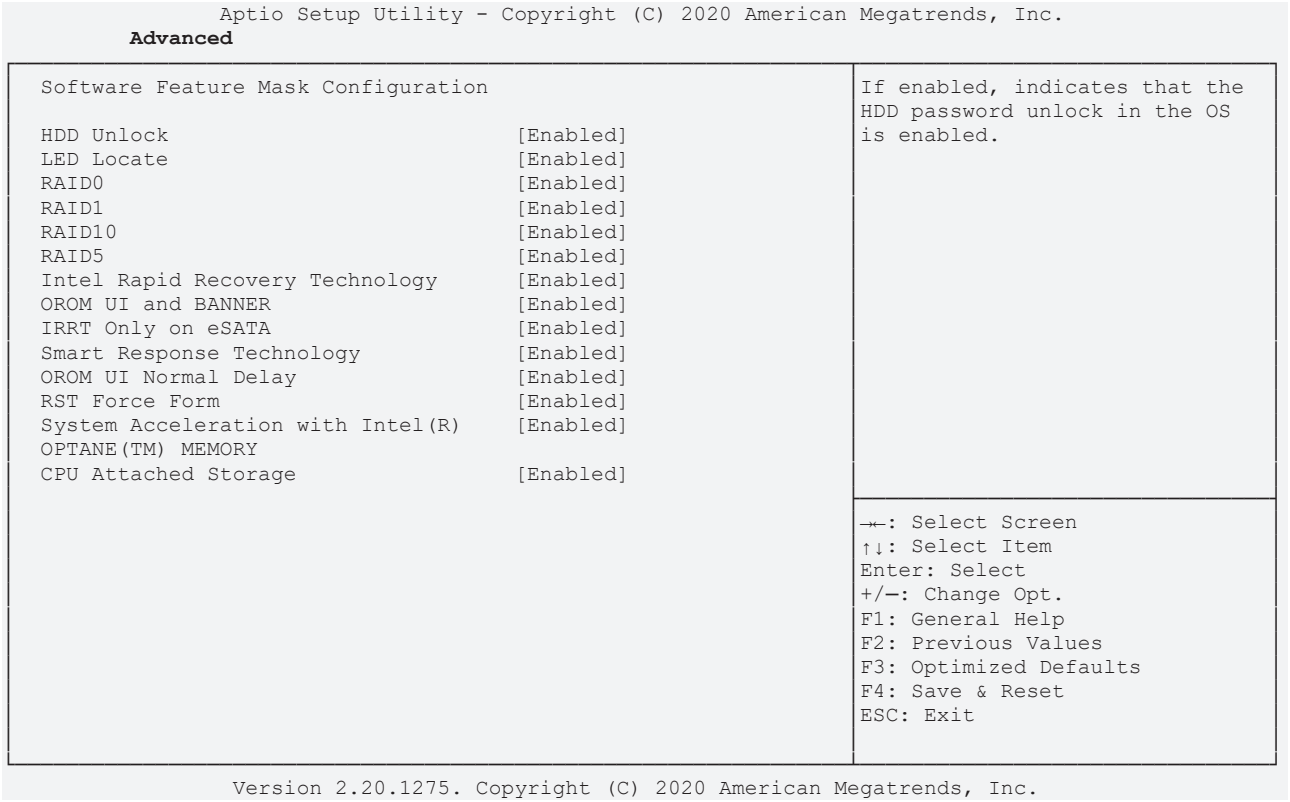
Bios entry	Options
SATA And RST Configuration	
SATA controller(s)	Enabled/Disabled
SATA Mode Selection	AHCI
SATA Test Mode	Disabled/Enabled
Software Feature Mask Configuration	Submenu see: Software Feature Mask Configuration [▶ 57]
Aggressive LPM support	Disabled/Enabled
Serial ATA port 0 - 5	None
Software Preserve	None
Port 0	Disabled/Enabled
Hot Plug	Disabled/Enabled
Configured as eSATA	None
External	Disabled/Enabled
Spin Up Device	Disabled/Enabled
SATA Device Type	HDD/SSD
SATA Port 0 DevSlp	Disabled/Enabled
DITO Configuration	Disabled/Enabled

NOTE

Settings on SATA ports 0-5

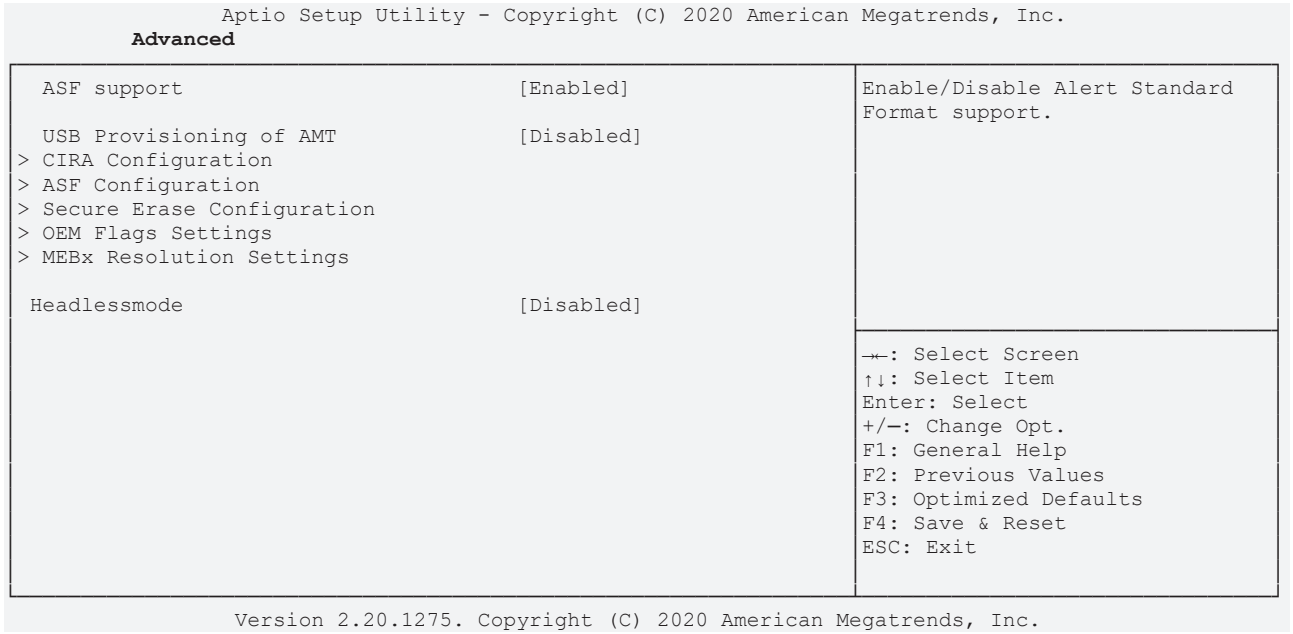
The possible settings on SATA ports 0-5 are identical. Therefore, these are summarized in the illustration.

8.3.14.1 Software Feature Mask Configuration



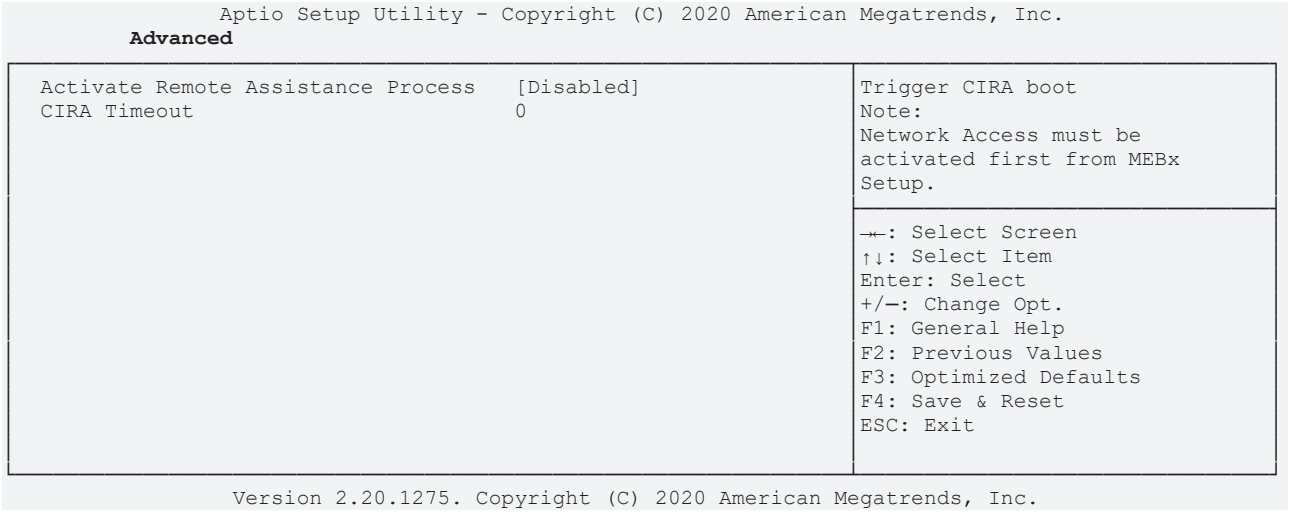
Bios entry	Options
Software Feature Mask Configuration	
HDD Unlock	Enabled/Disabled
LED Locate	Enabled/Disabled
RAID0	Enabled/Disabled
RAID1	Enabled/Disabled
RAID10	Enabled/Disabled
RAID5	Enabled/Disabled
Intel Rapid Recovery Technology	Enabled/Disabled
OROM UI and BANNER	Enabled/Disabled
IRRT Only on eSATA	Enabled/Disabled
Smart Response Technology	Enabled/Disabled
OROM UI Normal Delay	2, 4, 6, 8 secs
RST Force Form	Disabled/Enabled
System Acceleration with Intel(R)	Enabled/Disabled
Optane (TM) Memory	
CPU Attached Storage	Enabled/Disabled

8.3.15 AMT Configuration



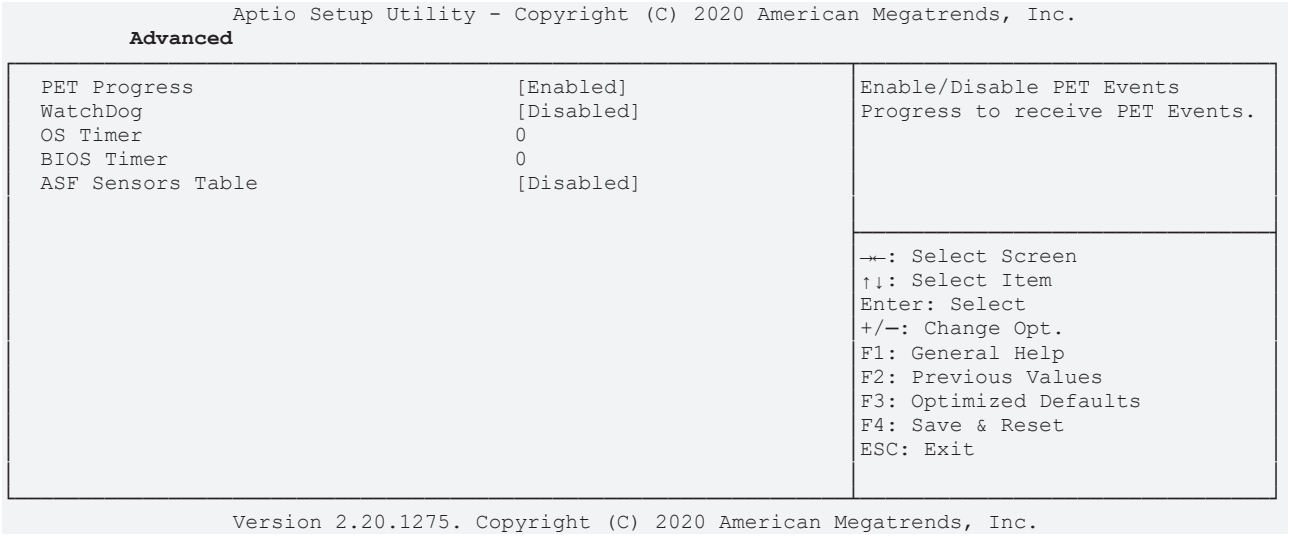
Bios entry	Options
ASF Support	Disabled/Enabled
USB Provisioning of AMT	Disabled/Enabled
CIRA Configuration	Submenu see: CIRA Configuration [▶ 59]
ASF Configuration	Submenu see: ASF Configuration [▶ 60]
Secure Erase Configuration	Submenu see: Secure Erase Configuration [▶ 60]
OEM Flags Settings	Submenu see: OEM Flags Settings [▶ 61]
MEBx Resolution Settings	Submenu see: MEBx Resolution Settings [▶ 62]
Headless mode	Disabled/Enabled

8.3.15.1 CIRA Configuration



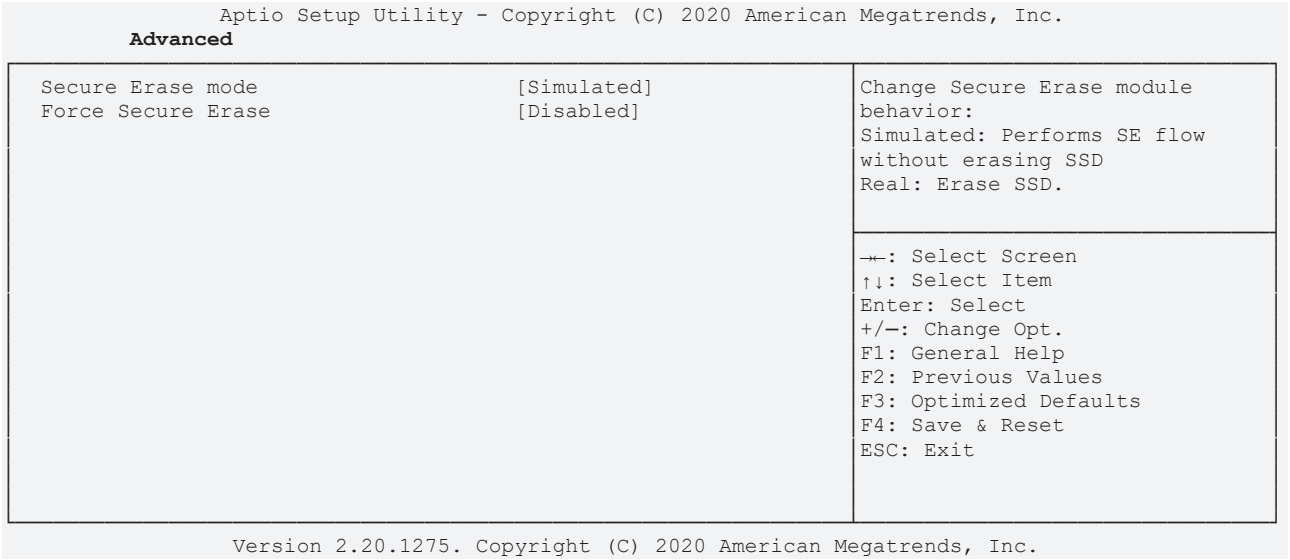
Bios entry	Options
Activate Remote Assistance Process	Disabled / Enabled
CIRA Timeout	None

8.3.15.2 ASF Configuration



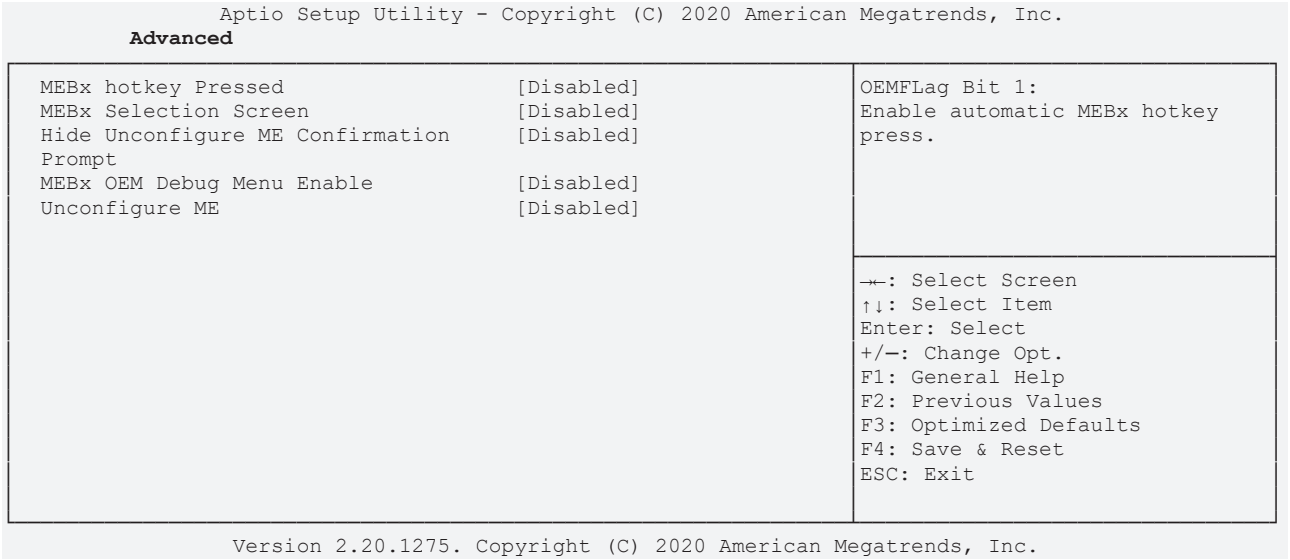
Bios entry	Options
PET Progress	Enabled/Disabled
WatchDog	Disabled/Enabled
OS Timer	None
BIOS Timer	None
ASF Sensors Table	Disabled/Enabled

8.3.15.3 Secure Erase Configuration



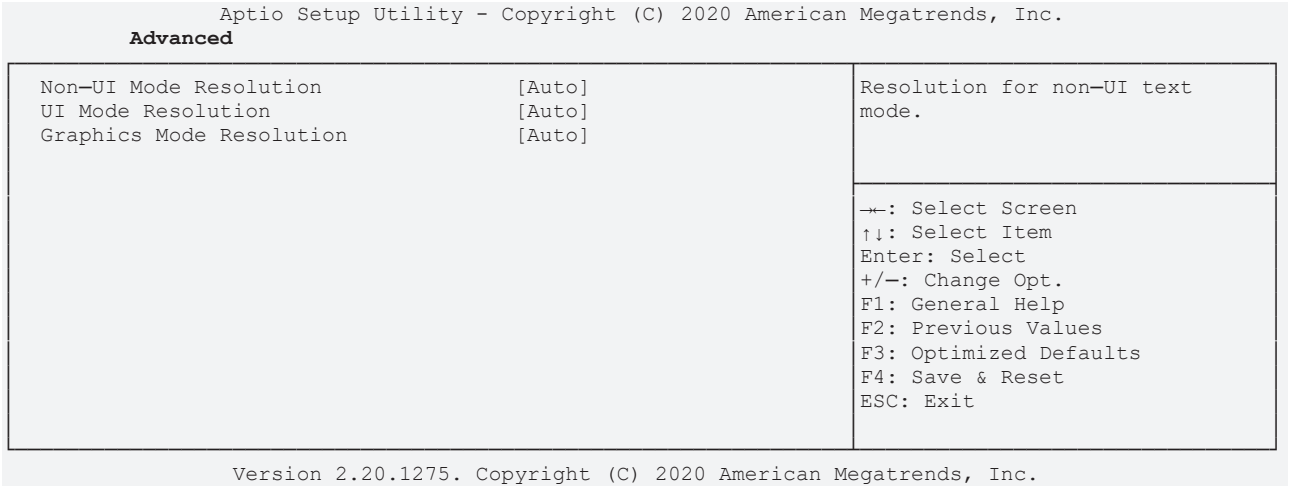
Bios entry	Options
Secure Erase Mode	Simulated/Real
Force Secure Erase	Disabled/Enabled

8.3.15.4 OEM Flags Settings



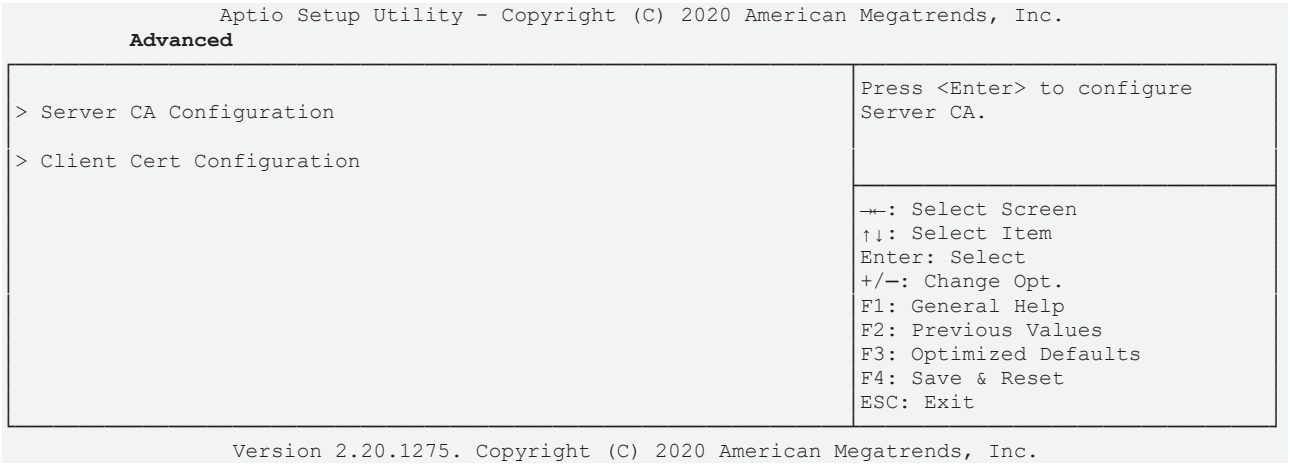
Bios entry	Options
MBEx hotkey Pressed	Disabled/Enabled
MBEx Selection Screen	Disabled/Enabled
Hide Unconfigure ME Confirmation Prompt	Disabled/Enabled
MBEx OEM Debug Menu Enable	Disabled/Enabled
Unconfigure ME	Disabled/Enabled

8.3.15.5 MEBx Resolution Settings



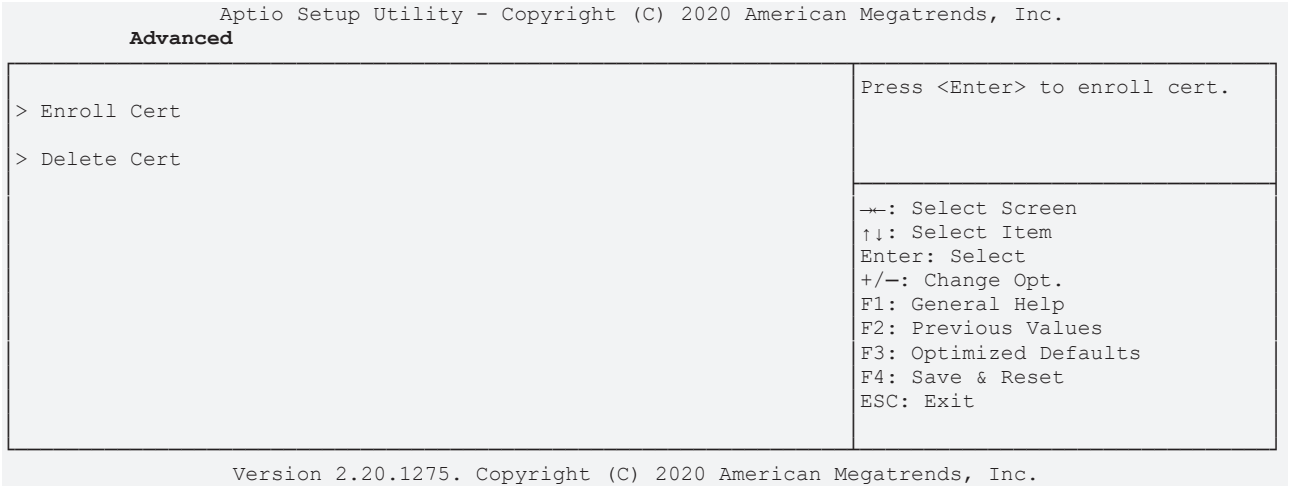
Bios entry	Options
Non-UI Resolution	Auto/80x25/100x31
UI Mode Resolution	Auto/80x25/100x31
Graphics Mode Resolution	Auto/640x480/800x600/1024x768

8.3.16 TLs Auth Configuration



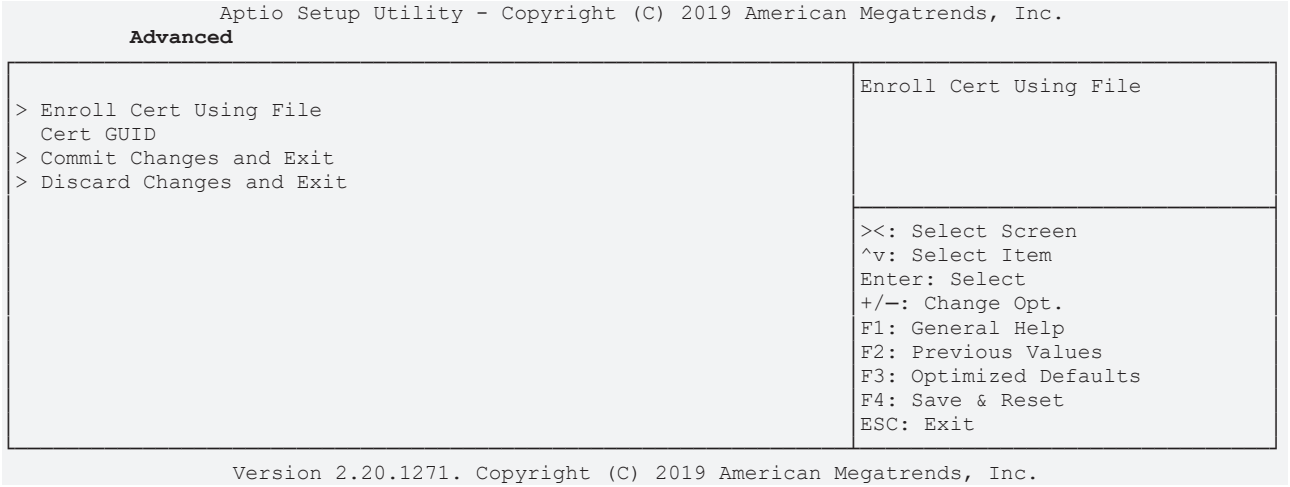
Bios entry	Options
Server CA Configuration	Submenu see: Server CA Configuration [▶ 63]
Client Cert Configuration	None

8.3.16.1 Server CA Configuration



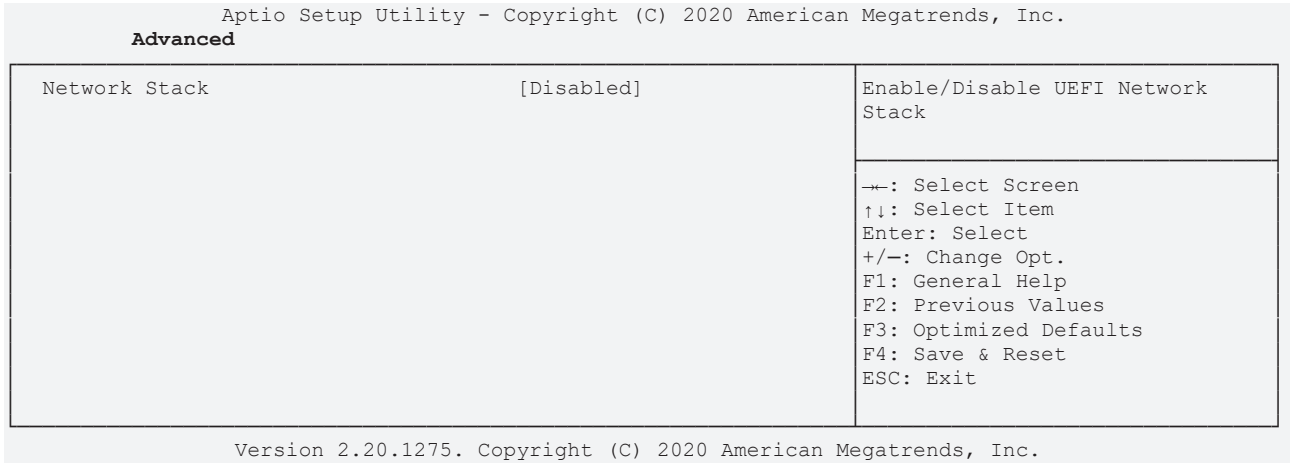
Bios entry	Options
Enroll Cert	Submenu see: Enroll Cert [▶ 63]
Delete Cert	None

8.3.16.1.1 Enroll Cert



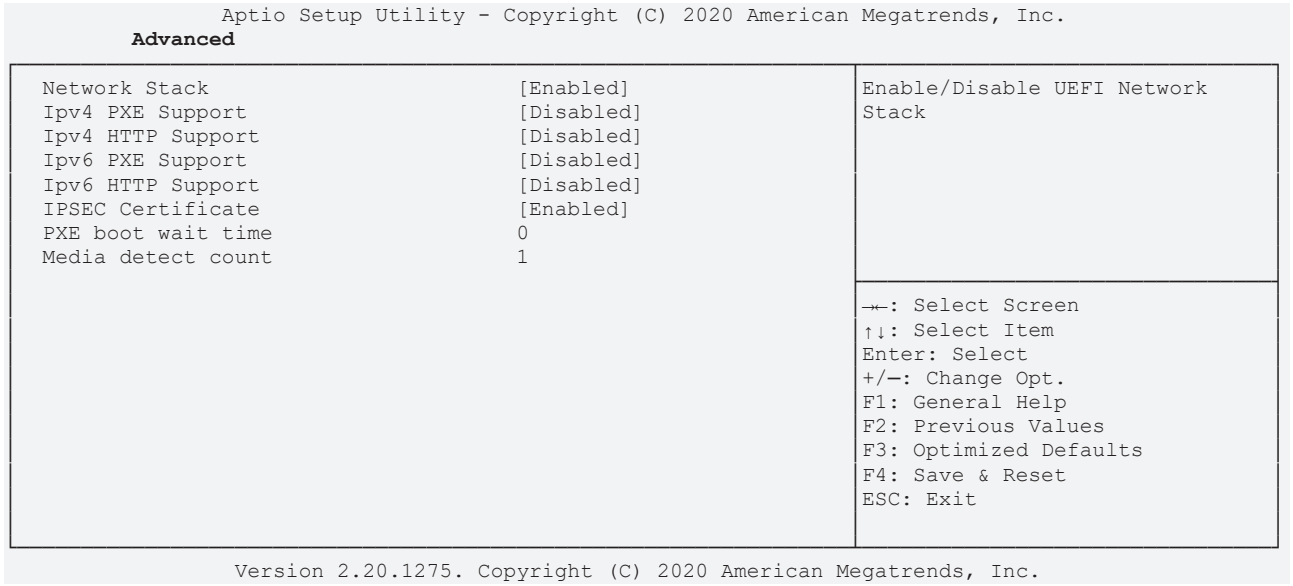
Bios entry	Options
Enroll CertEnroll Cert Using File	None
Cert GUID	None
Commit Changes and Exit	None
Discard Changes and Exit	None

8.3.17 Network Stack Configuration



Bios entry	Options
Network Stack	Disabled/Enabled

8.3.18 Network Stack Configuration enabled



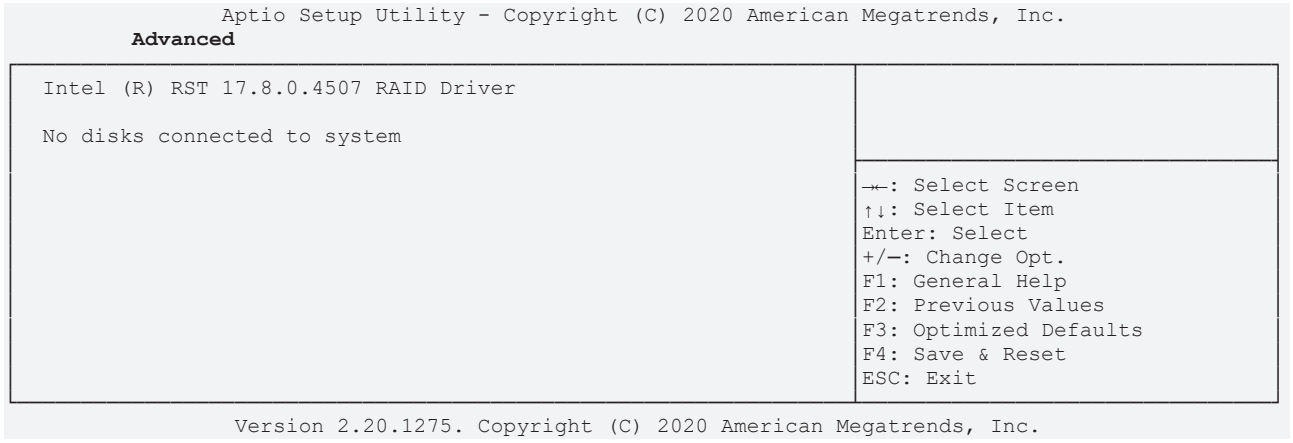
Bios entry	Options
Network Stack	Enabled/Disabled
Ipv4 PXE Support	Disabled/Enabled
Ipv4 HTTP Support	Disabled/Enabled
Ipv6 PXE Support	Disabled/Enabled
Ipv6 HTTP Support	Disabled/Enabled
IPSEC Certificate	Enabled/Disabled
PXE boot wait time	None
Media detect count	None

NOTE

PXE Boot available

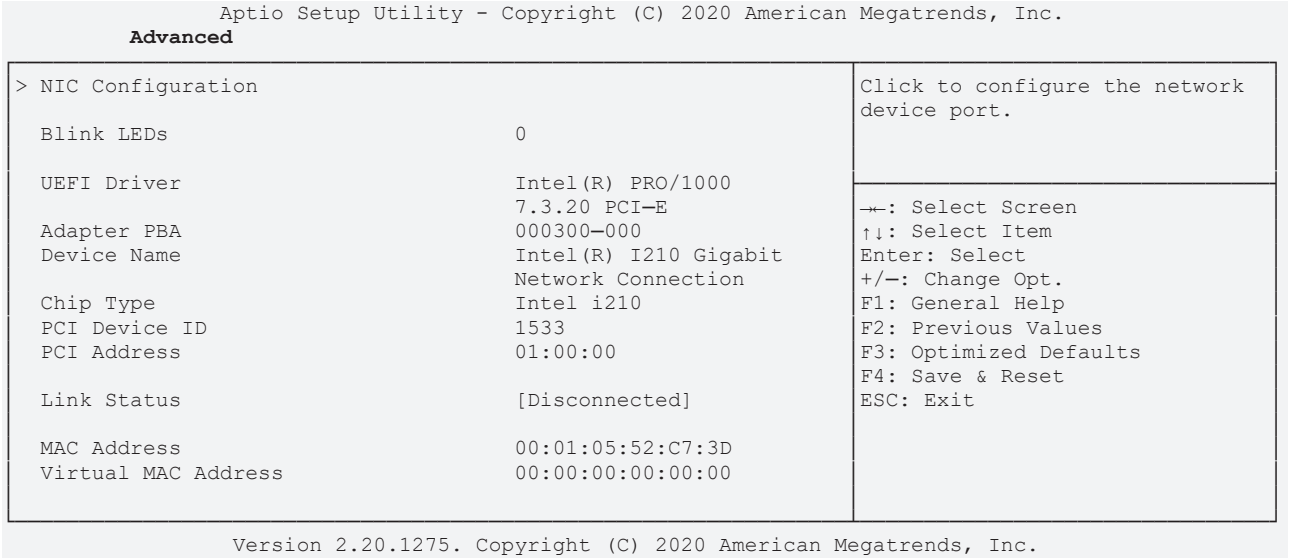
PXE Boot is available if you set Network Stack and Ipv4 PXE support to "Enable".

8.3.19 Intel Rapid Storage Technology



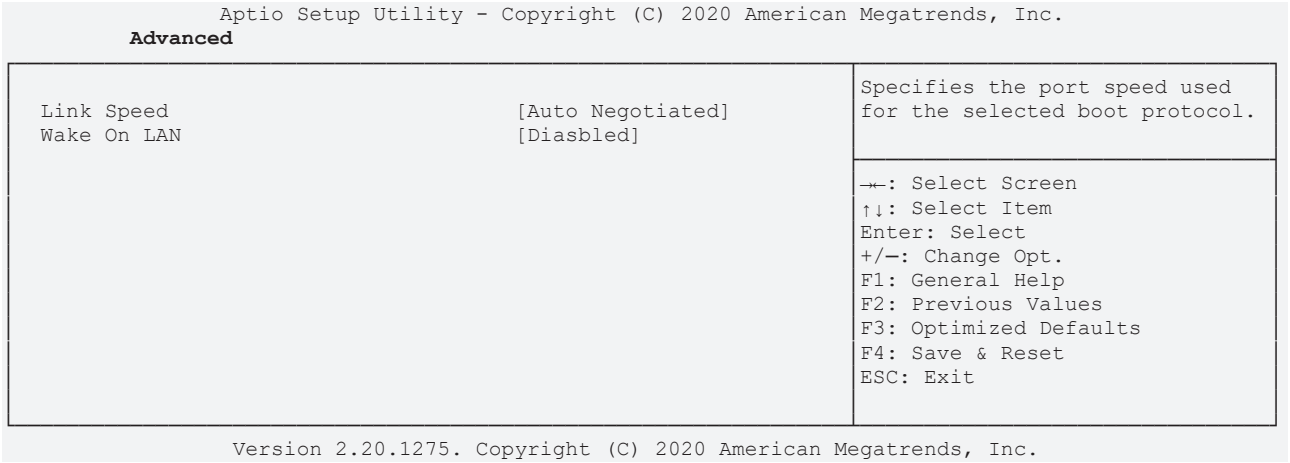
Bios entry	Options
Intel® RST 17.8.0.4507 RAID Driver	
No disks connected to system	None

8.3.20 Intel I210 Gigabit Network Connection



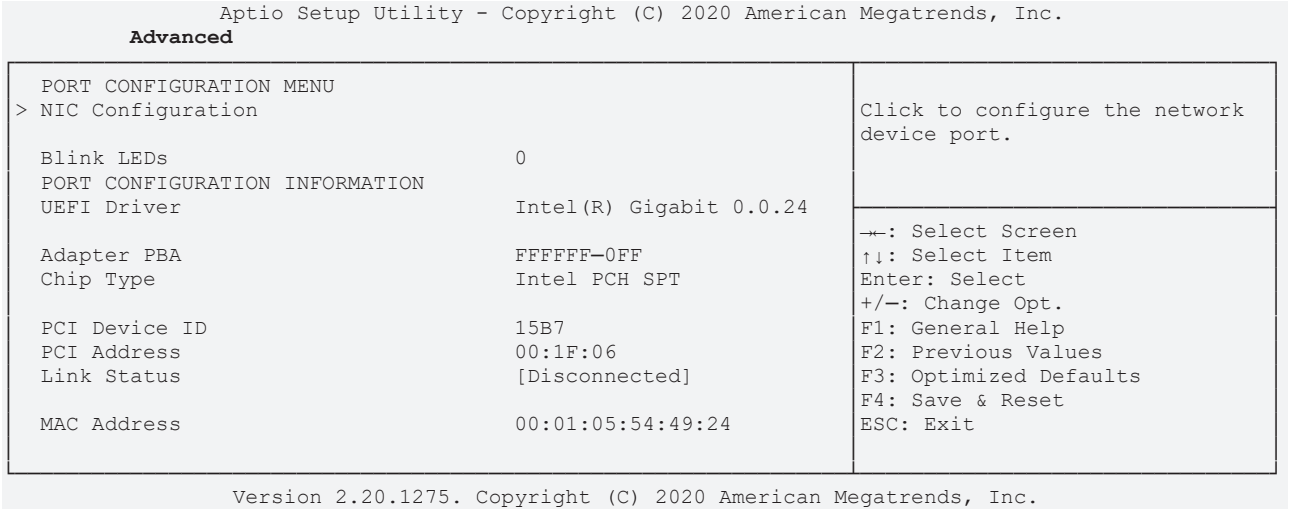
Bios entry	Options
NIC Configuration	Submenu see: NIC Configuration [▶ 68]
Flashing LEDs	None
UEFI driver	None
PBA adapter	None
Device Name	None
Chip type	None
PCI Device ID	None
PCI Address	None
Link status	None
MAC Address	None
Virtual MAC Address	None

8.3.20.1 NIC Configuration



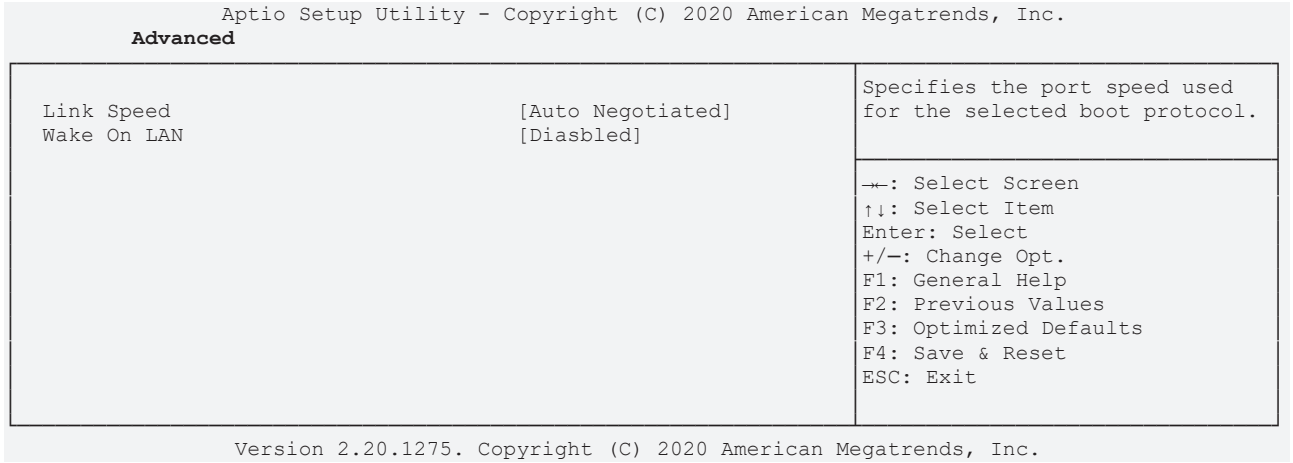
Bios entry	Options
Link Speed	Auto Negotiated/10 Mbps Half/10 Mbps Full/ 100 Mbps Half/100 Mbps Full
Wake On LAN	Disabled/Enabled

8.3.21 Intel Ethernet Connection(2) I219-LM



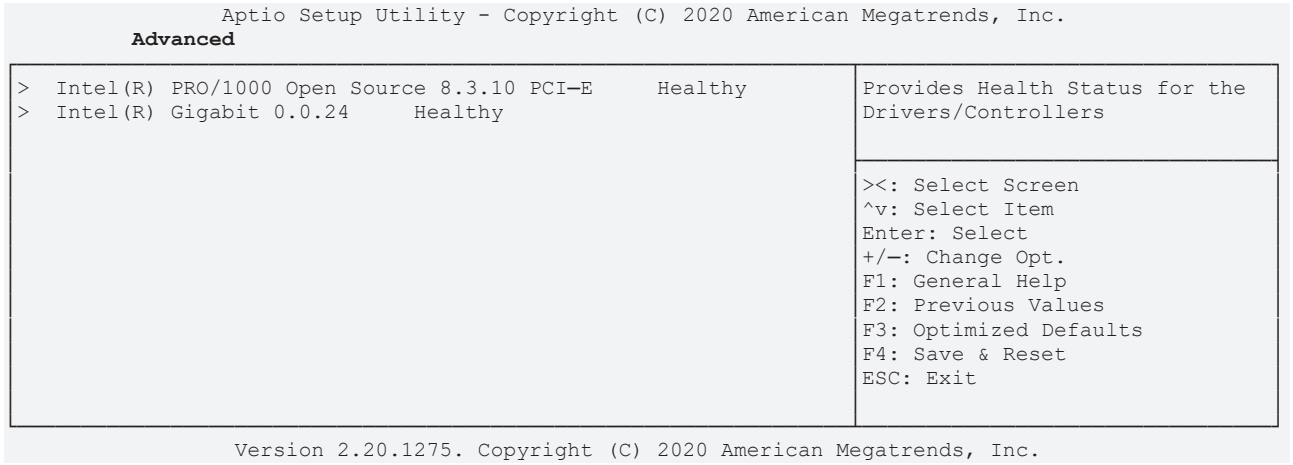
Bios entry	Options
PORT CONFIGURATION MENU	
NIC Configuration	See submenu: NIC Configuration [▶ 70]
Flashing LEDs	None
PORT CONFIGURATION INFORMATION	
UEFI driver	None
PBA adapter	None
Chip type	None
PCI Device ID	None
PCI Address	None
Link status	None
MAC Address	None

8.3.21.1 NIC Configuration



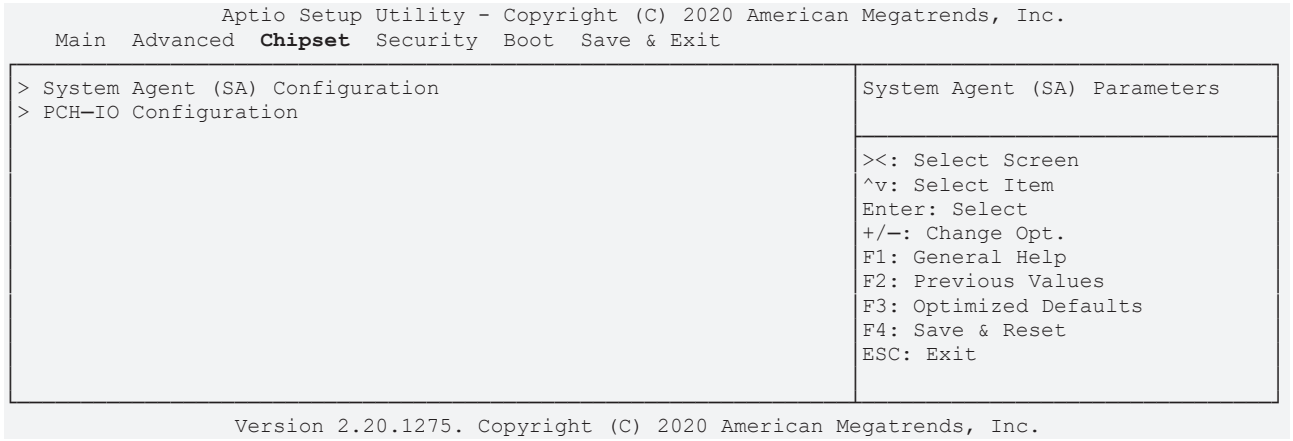
Bios entry	Options
Link Speed	Auto Negotiated/10 Mbps Half/10 Mbps Full/ 100 Mbps Half/100 Mbps Full
Wake On LAN	Disabled/Enabled

8.3.22 Driver Health



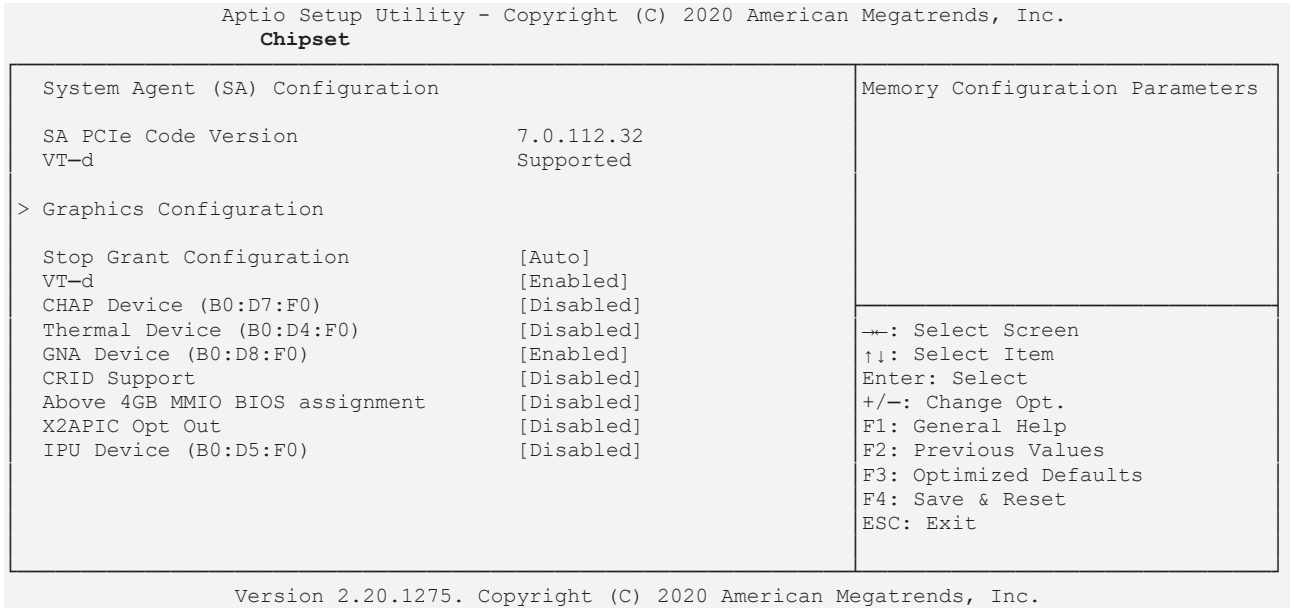
Bios entry	Options
Intel(R) PRO/1000 Open Source 8.3.10 PCI-E Healthy	None
Intel(R) Gigabit 0.0.24 Healthy	None

8.4 Chipset



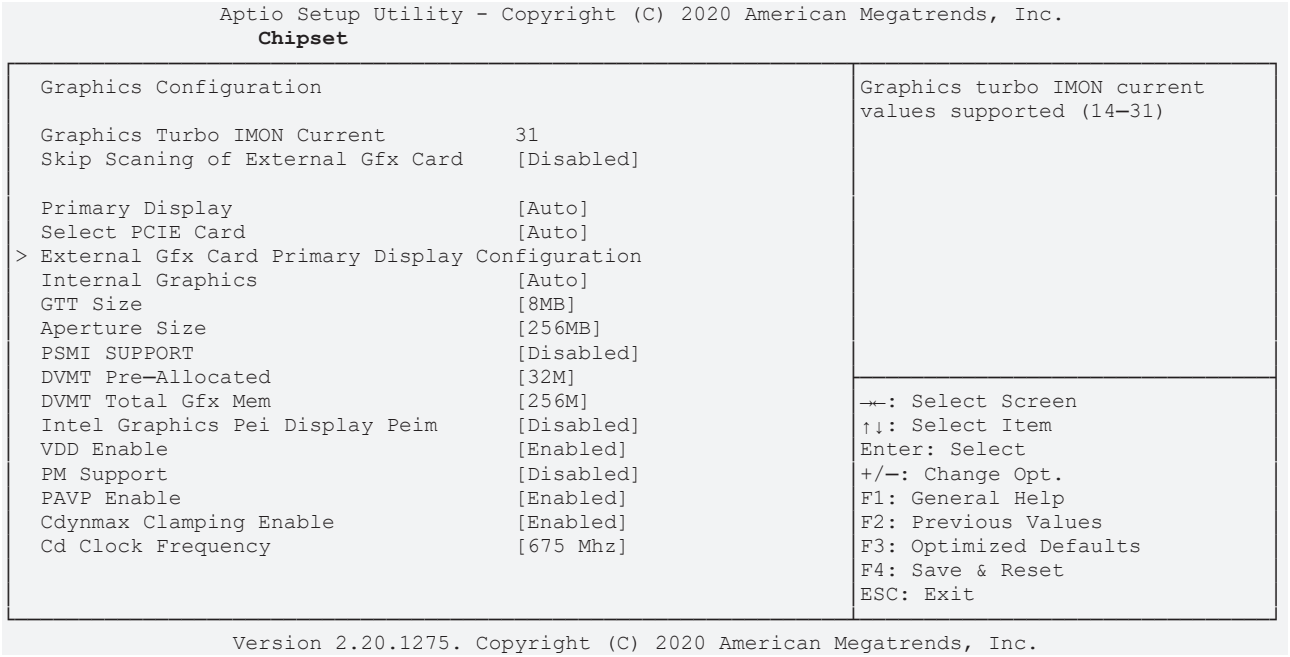
Bios entry	Options
System Agent (SA) Configuration	Submenu see: System Agent (SA) Configuration [▶ 73]
PCH-IO Configuration	Submenu see: PCH-IO Configuration [▶ 75]

8.4.1 System Agent (SA) Configuration



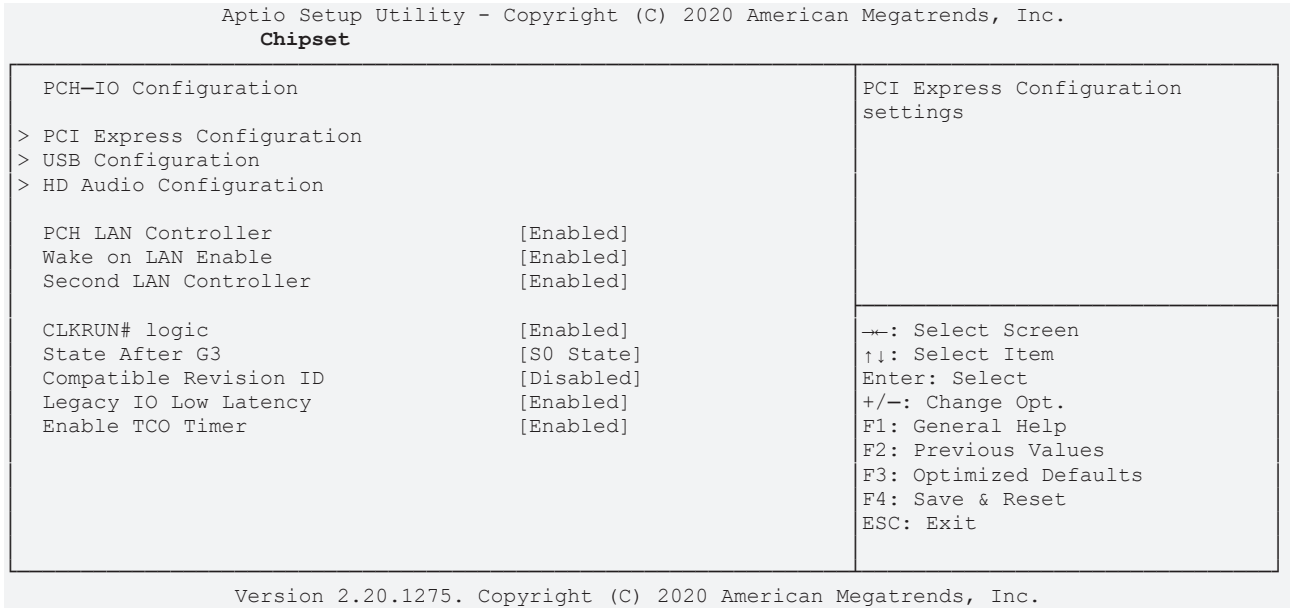
Bios entry	Options
System Agent (SA) Configuration	
SA PCIe code version	None
VT-d	None
Graphics Configuration	Submenu see: Graphics Configuration [▶ 74]
Stop grant configuration	Auto/Manual
VT-d	Enabled/Disabled
CHAP device (B0:D7:F0)	Disabled/Enabled
Thermal device (B0:D4:F0)	Enabled/Disabled
GNA device (B0:D8:F0)	Enabled/Disabled
CRID support	Disabled/Enabled
Above 4GB MMIO BIOS assignment	Disabled/Enabled
X2APIC Opt Out	Disabled/Enabled
IPU device (B0:D5:F0)	Disabled/Enabled

8.4.1.1 Graphics Configuration



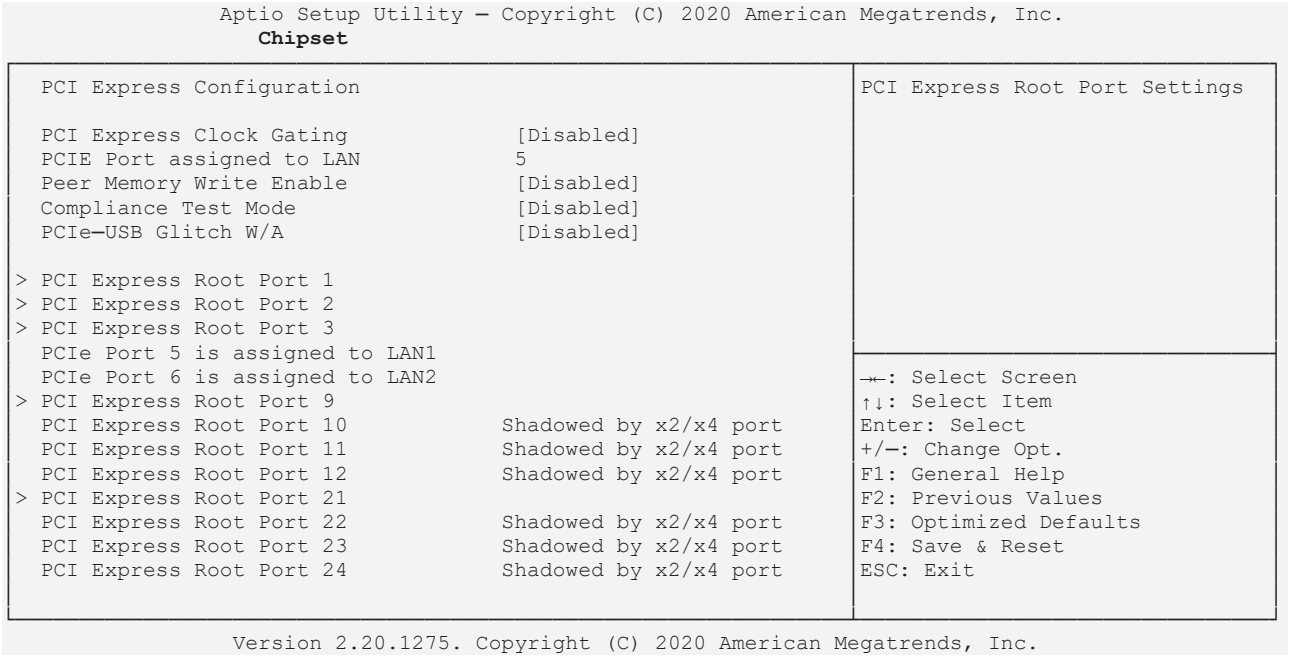
Bios entry	Options
Graphics Configuration	
Graphics Turbo IMON Current	None
Skip Scanning of External Gfx Card	Disabled/Enabled
Primary Display	Auto/IGFX/PCI/SG
Select PCIE Card	Auto/Elk Creek 4/PEG Eval
External Gfx Card Primary Display Configuration	None
Internal Graphics	Auto/Disabled/Enabled
GTT Size	2/4/8 MB
Aperture Size	128/256/512/1024/2048 MB
PSMI SUPPORT	Disabled/Enabled
DVMT Pre-Allocated	0M, 32M…60M
DVMT Total Gfx Mem	128M/256M/MAX
Intel Graphics Pei Display Peim	Disabled/Enabled
VDD Enable	Enabled/Disabled
PM Support	None
PAVP Enable	Enabled/Disabled
Cdynmax Clamping Enable	Enabled/Disabled
Cd Clock Frequency	337.5/450/540/675 Mhz

8.4.2 PCH-IO Configuration



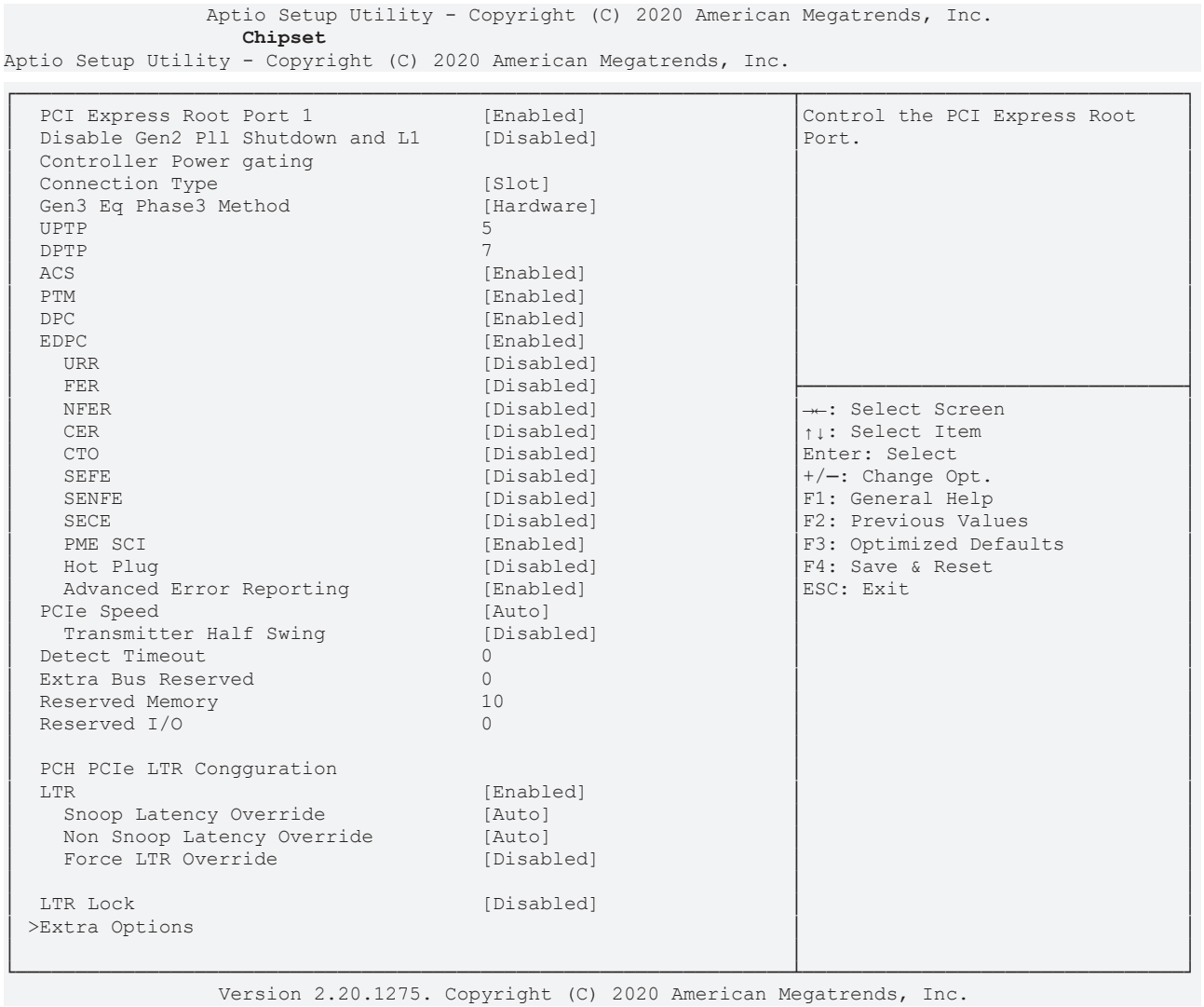
BIOS entry	Options
PCH-IO Configuration	
PCI Express Configuration	Submenu see: PCI Express Configuration (Q370) [▶ 76]
USB Configuration	Submenu see: USB Configuration [▶ 80]
HD Audio Configuration	Submenu see: HD Audio Configuration [▶ 80]
PCH LAN Controller	Enabled/Disabled
Wake on LAN Enable	Enabled/Disabled
Second LAN Controller	Enabled/Disabled
PS_ON Enable	Disabled/Enabled
CLKRUN# logic	Enabled/Disabled
State After G3	S0 state/S5 state
Compatible Revision ID	None
Legacy IO Low Latency	Enabled/Disabled
Enable TCO Timer	Disabled/Enabled

8.4.2.1 PCI Express Configuration (Q370)



Bios entry	Options
PCI Express Configuration	
PCI Express Clock Gating	Disabled/Enabled
PCIE port assigned to LAN	None
Peer Memory Write Enable	Disabled/Enabled
Compliance Test Mode	Disabled/Enabled
PCIe USB Glitch W/A	Disabled/Enabled
PCI Express Root Port 1	See submenu: PCI Express Root Port 1 [▶ 77]
PCI Express Root Port 2	See submenu: PCI Express Root Port 1 [▶ 77]
PCI Express Root Port 3	See submenu: PCI Express Root Port 1 [▶ 77]
PCIe Port 5 is assigned to LAN1	None
PCIe Port 6 is assigned to LAN2	None
PCI Express Root Port 9	See submenu: PCI Express Root Port 1 [▶ 77]
PCI Express Root Port 10	None
PCI Express Root Port 11	None
PCI Express Root Port 12	None
PCI Express Root Port 21	See submenu: PCI Express Root Port 1 [▶ 77]
PCI Express Root Port 22	None
PCI Express Root Port 23	None
PCI Express Root Port 24	None

8.4.2.1.1 PCI Express Root Port 1



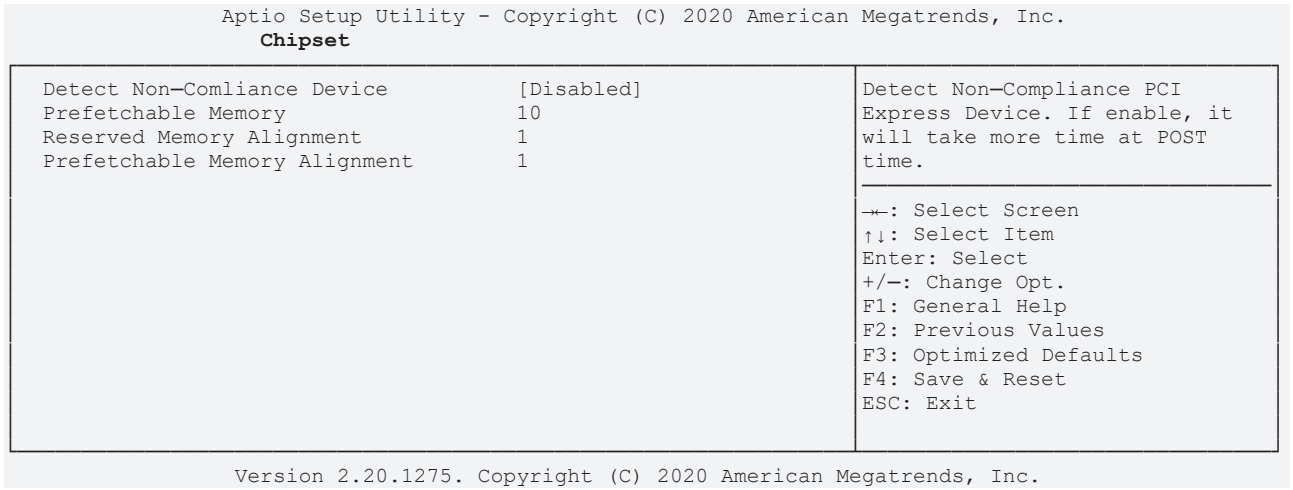
BIOS entry	Options
PCI Express Root Port 1	Disabled/Enabled
Disable Gen2 Pll Shutdown and L1 and Controller Power gating	Disabled/Enabled
Connection type	Built-in/Slot
Gen3 Eq Phase3 Method	Hardware/Static Coeff.
UPTP	None
DPTP	None
ACS	Enabled/Disabled
PTM	Enabled/Disabled
DPC	Enabled/Disabled
EDPC	Enabled/Disabled
URR	Disabled/Enabled
FER	Disabled/Enabled
NFER	Disabled/Enabled
CER	Disabled/Enabled
CTO	Disabled/Enabled
SEFE	Disabled/Enabled
SENFE	Disabled/Enabled
PME SCI	Enabled/Disabled
Hot Plug	Disabled/Enabled
Advanced Error Reporting	Enabled/Disabled
PCIe Speed	Auto/Gen1/Gen2/Gen3
Transmitter Half Swing	Disabled/Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled/Disabled
Snoop Latency Override	Disabled/Manual/Auto
Non Snoop Latency Override	Disabled/Manual/Auto
Force LTR Override	Disabled/Enabled
LTR Lock	Disabled/Enabled
Extra Options	Submenu see: Extra Options [▶ 79]

NOTE

PCI Express Configuration

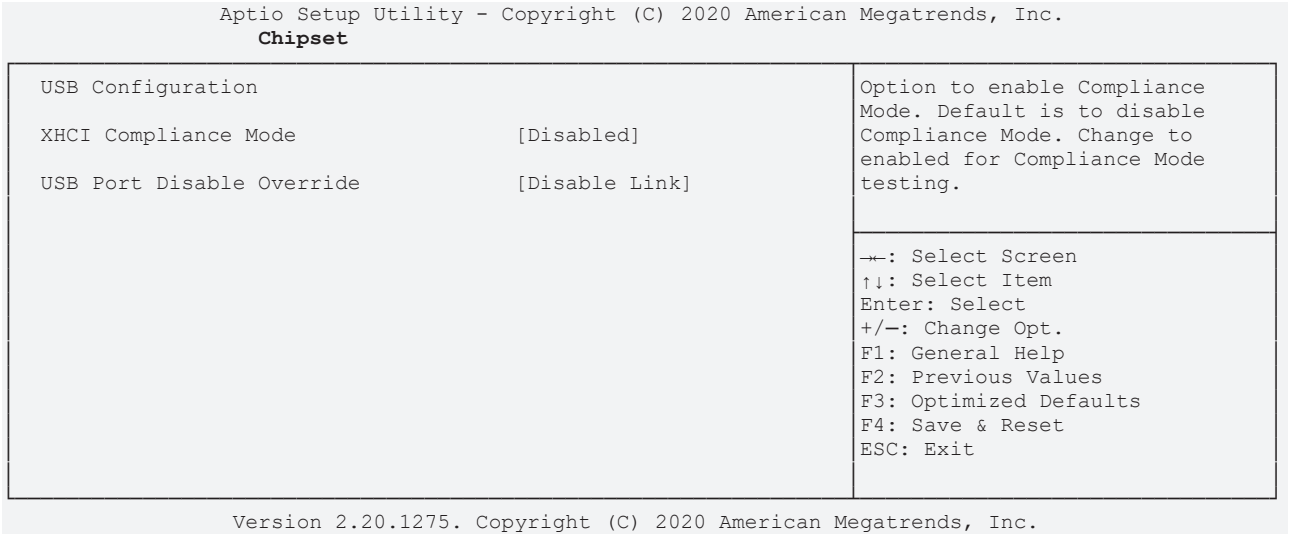
The BIOS entries and options on ports 1-3, 9 and 21 are identical. Port 1 is shown as an example

8.4.2.1.1.1 Extra Options



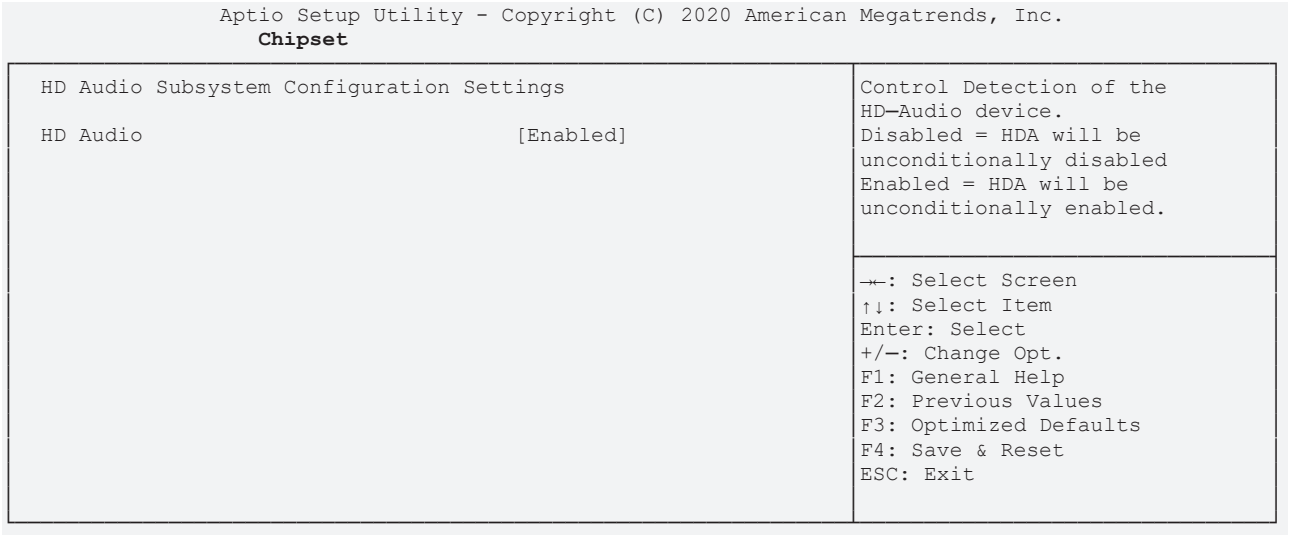
BIOS entry	Options
Detect non-compliance device	Disabled/Enabled
Prefetchable Memory	None
Reserved Memory Alignment	None
Prefetchable Memory Alignment	None

8.4.2.2 USB Configuration



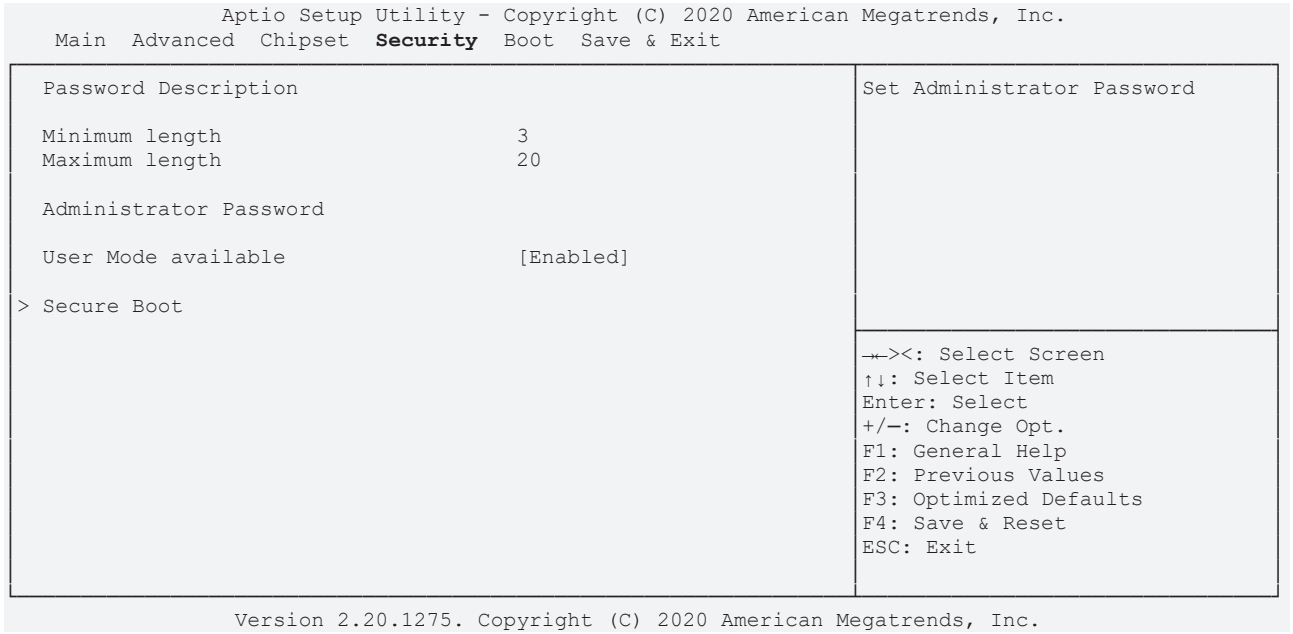
BIOS entry	Options
USB Configuration	
XHCI compliance mode	Disabled / Enabled
USB port disable override	Disable link / Select per-pin

8.4.2.3 HD Audio Configuration



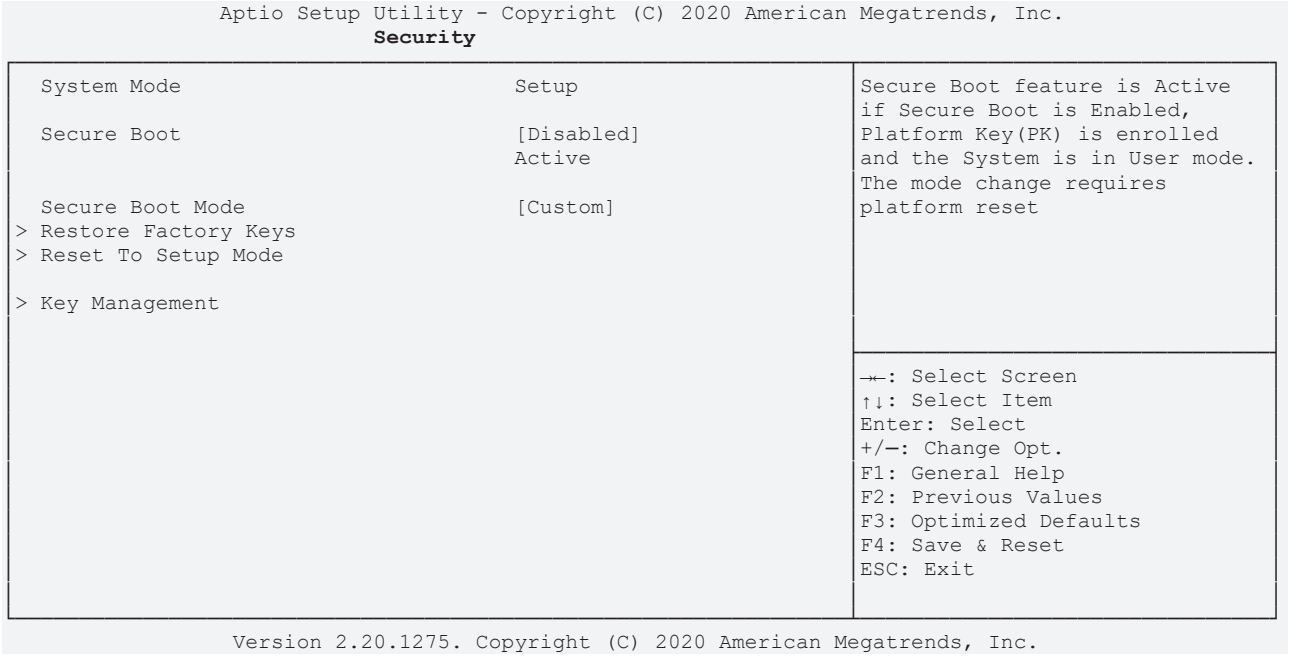
Bios entry	Options
HD Audio Subsystem Configuration Settings	
HD audio	Enabled/Disabled

8.5 Security



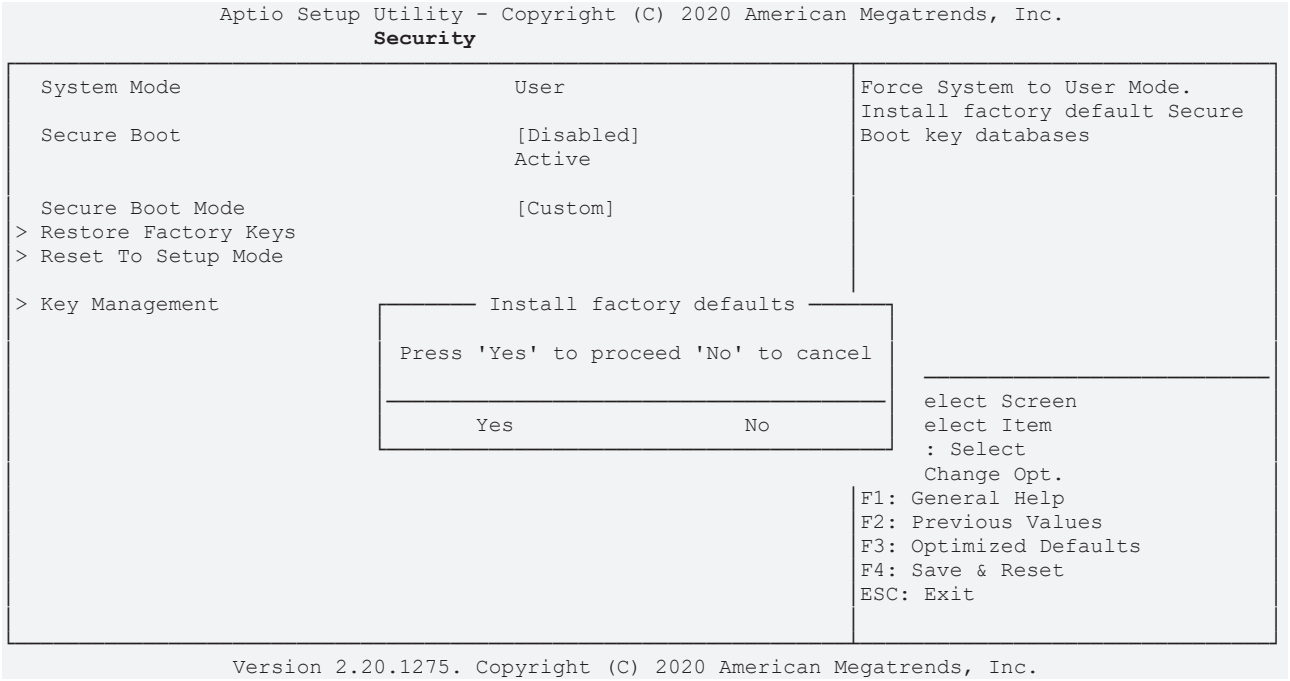
Setup entry	Options
Password Description	
Minimum length	None
Maximum length	None
Administrator Password	Here you can set an administrator password.
User Mode available	Enabled/Disabled
Secure Boot	Submenu see: Secure Boot [▶ 82]

8.5.1 Secure Boot



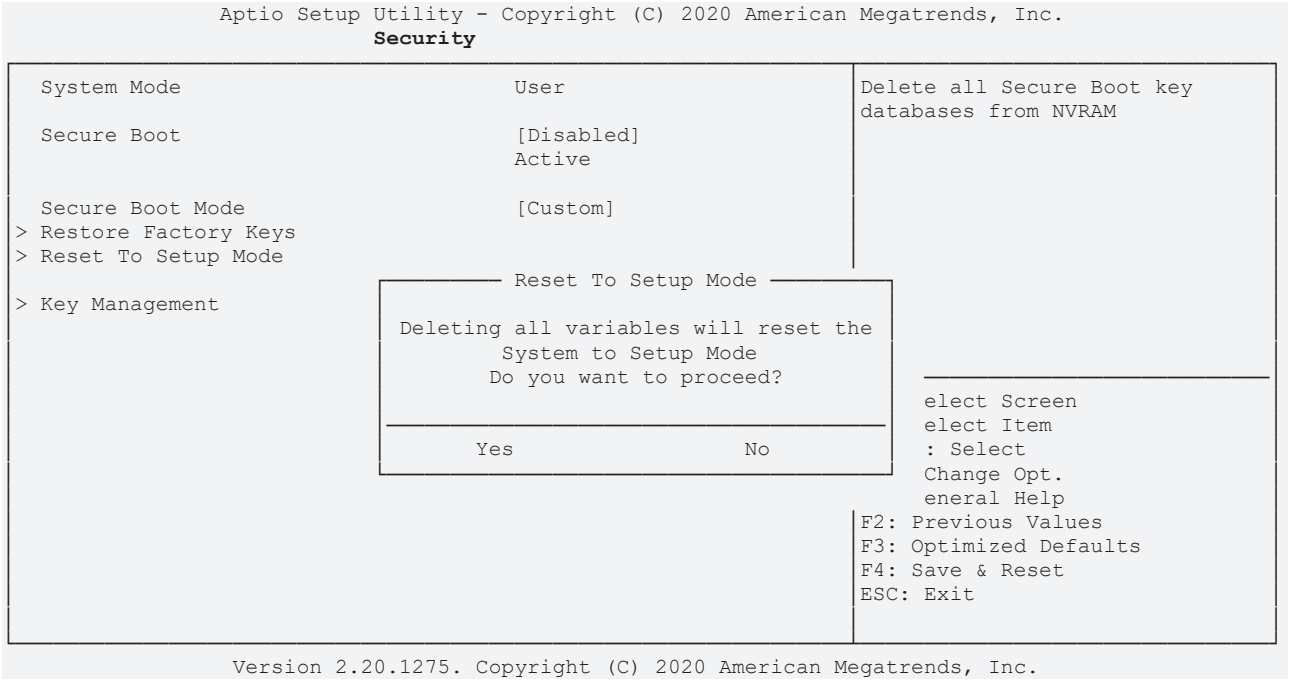
Bios entry	Options
System Mode	None
Secure Boot	Disabled/Enabled Active
Secure Boot Mode	Custom/Standard
Restore Factory Keys	Submenu see: Restore factory keys [▶ 83]
Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 84]
Key Management	Submenu see: Key Management [▶ 85]

8.5.1.1 Restore factory keys



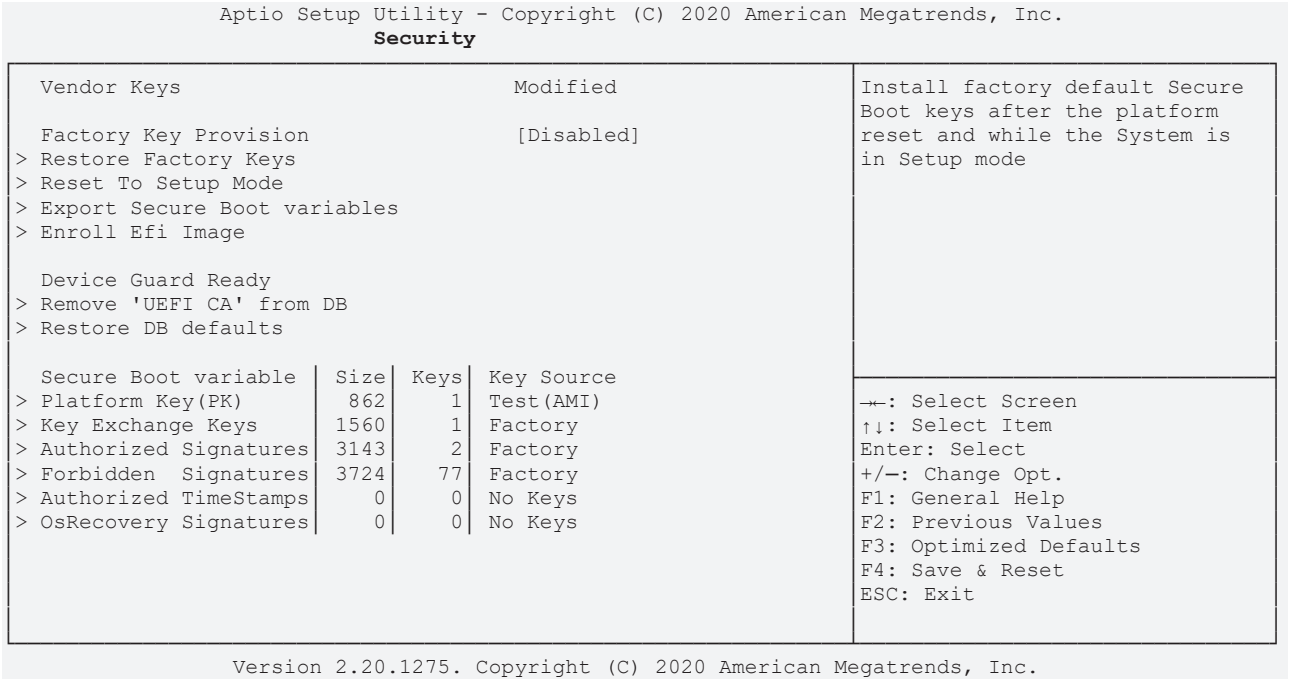
Bios entry	Options
System Mode	None
Secure Boot	Disabled/Enabled Active
Secure Boot Mode	Custom/Standard
Restore Factory Keys	Install factory defaults, see box

8.5.1.2 Reset To Setup Mode



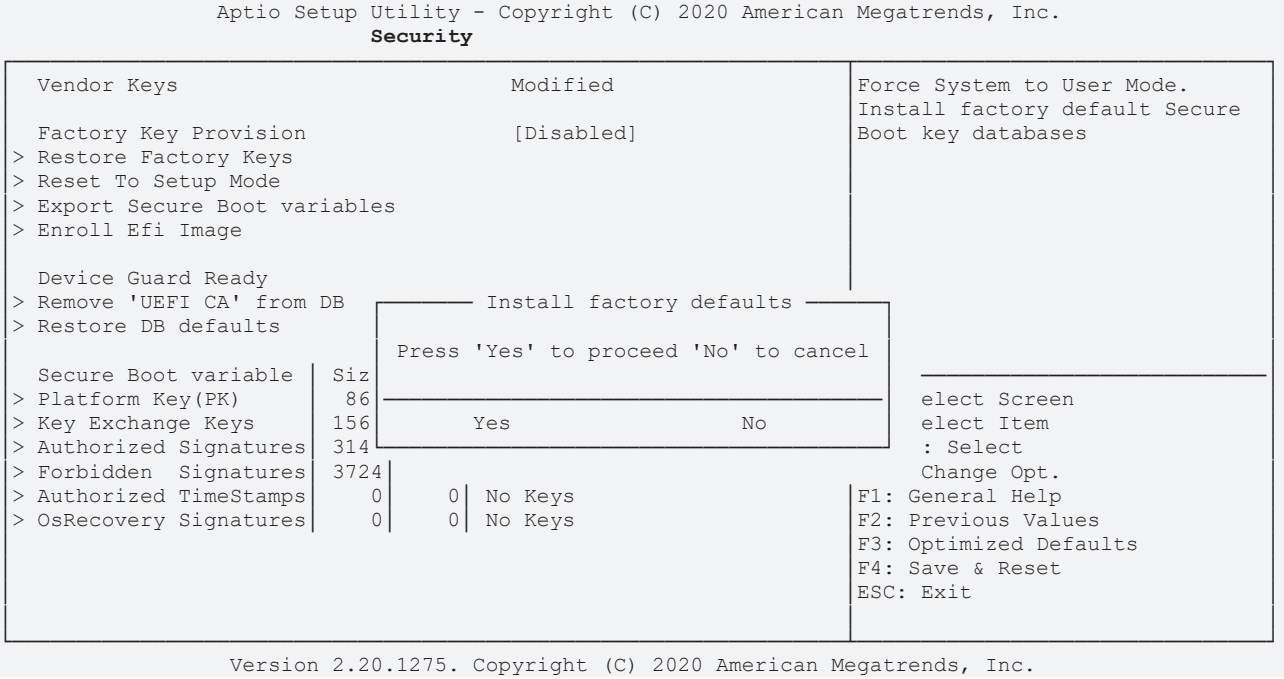
Bios entry	Options
System Mode	none
Secure Boot	Disabled/Enabled Active
Secure Boot Mode	Custom / Standard
Reset To Setup Mode	Reset To Setup Mode (see box)

8.5.1.3 Key Management



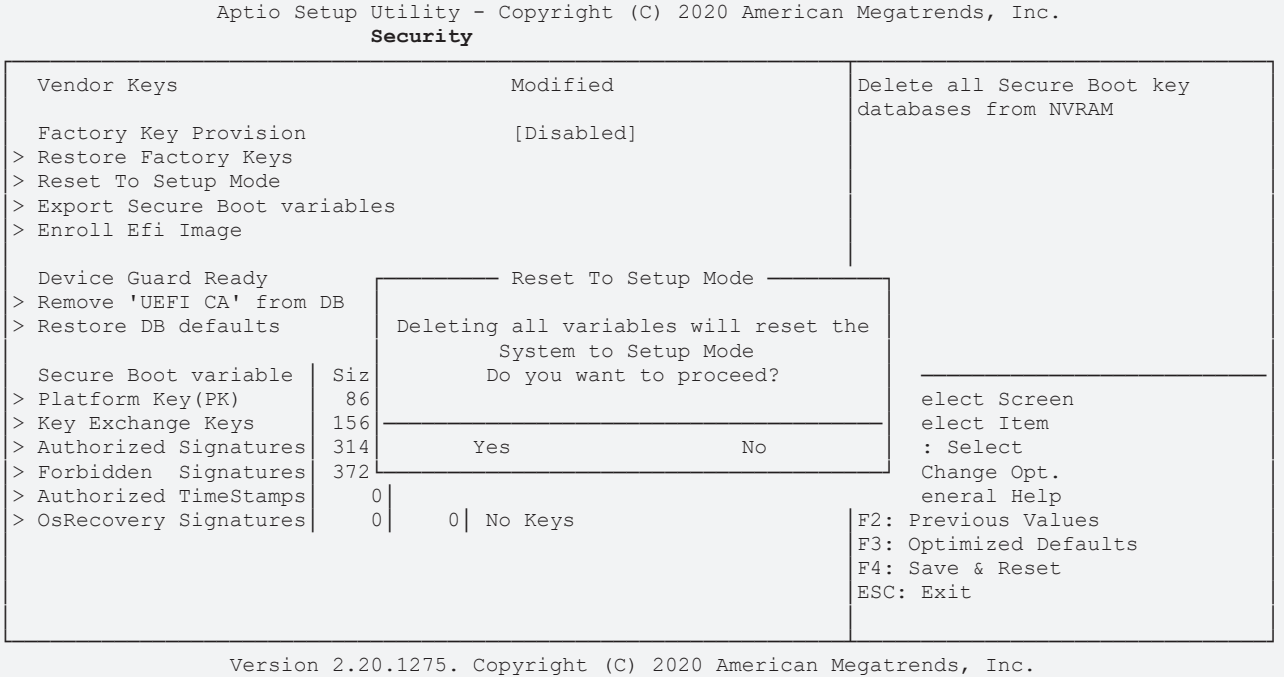
Bios entry	Options
Vendor Keys	None
Factory Key Provision	Disabled/Enabled
Restore Factory Keys	Submenu see: Restore Factory Keys [▶ 86]
Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 87]
Export Secure Boot variables	Submenu see: Export Secure Boot Variables [▶ 88]
Enroll Efi Image	Submenu see: Enroll Efi Image [▶ 89]
Device Guard Ready	
Remove 'UEFI CA' from DB	Submenu see: Remove UEFI CA from DB [▶ 89]
Restore DB defaults	Submenu see: Restore DB faults [▶ 90]
Secure Boot variable	
PlatformKey(PK)	Press enter key
Key Exchange Keys	Press enter key
Authorized Signatures	Press enter key
Forbidden Signatures	Press enter key
Authorized TimeStamps	Press enter key
OsRecovery Signatures	Press enter key

8.5.1.3.1 Restore Factory Keys



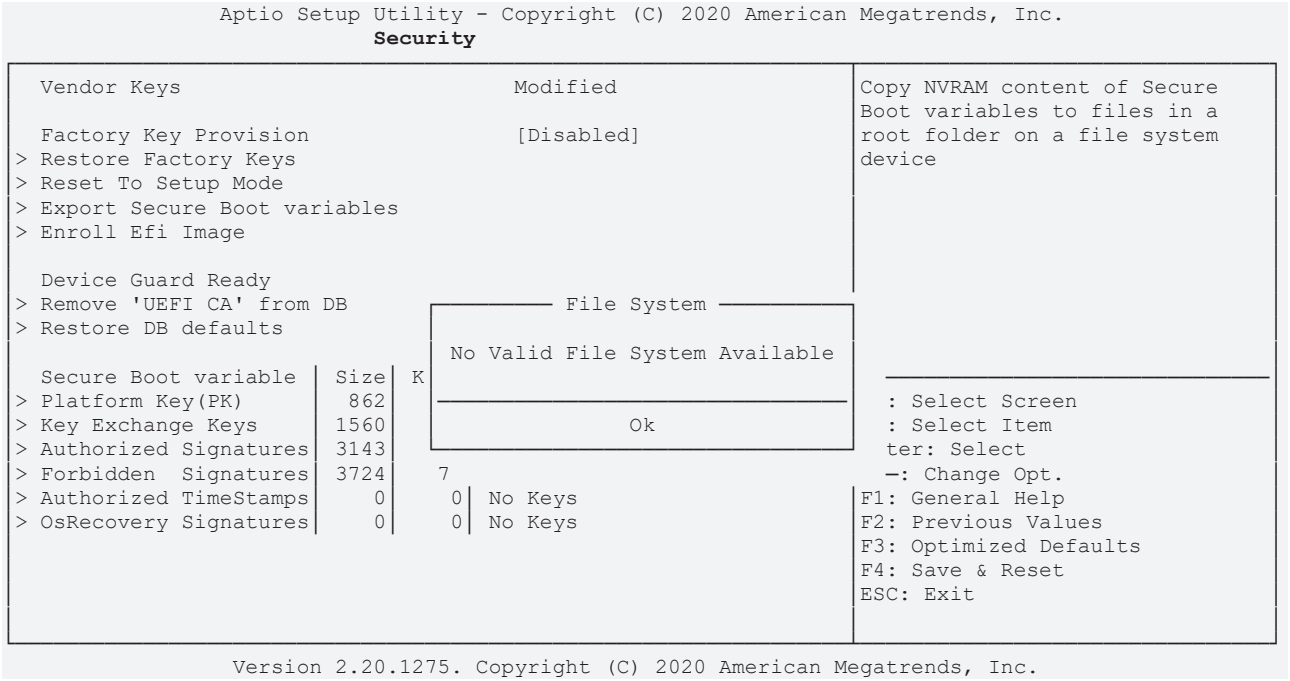
Bios entry	Options
Vendor Keys	None
Restore Factory Keys	Install factory defaults, see box

8.5.1.3.2 Reset To Setup Mode



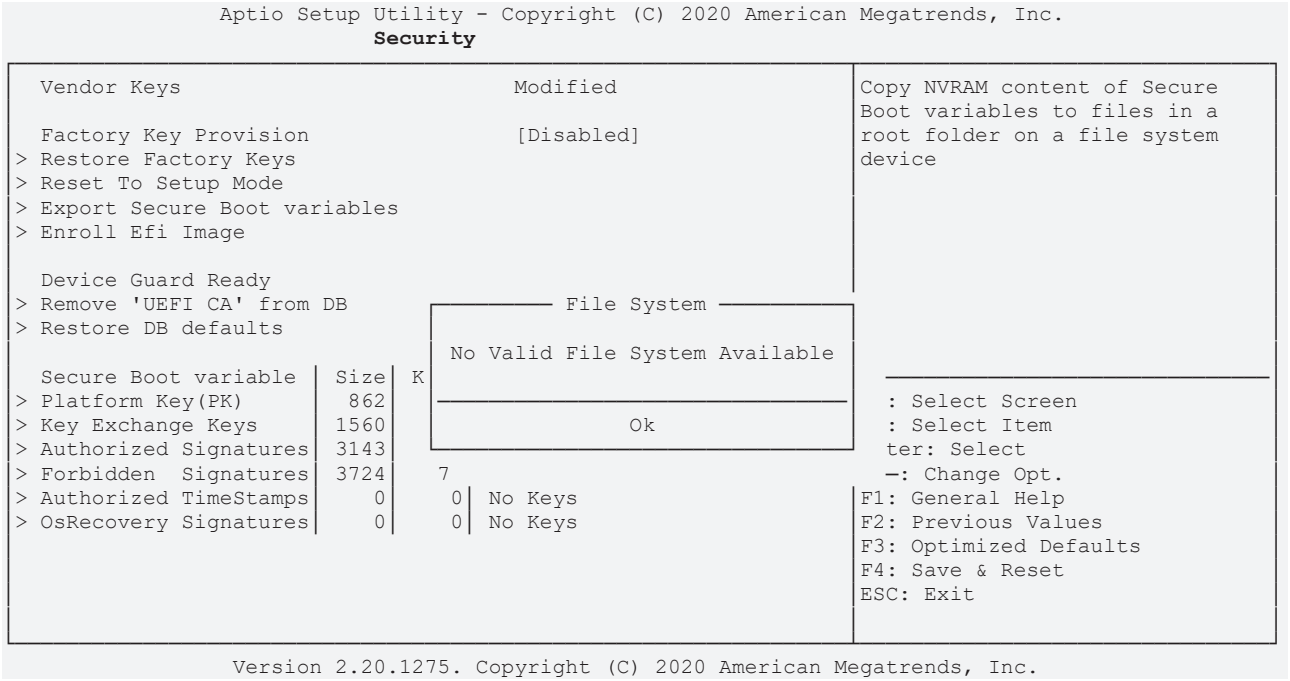
Bios entry	Options
Vendor Keys	None
Reset To Setup Mode	Reset To Setup Mode, see box

8.5.1.3.3 Export Secure Boot Variables



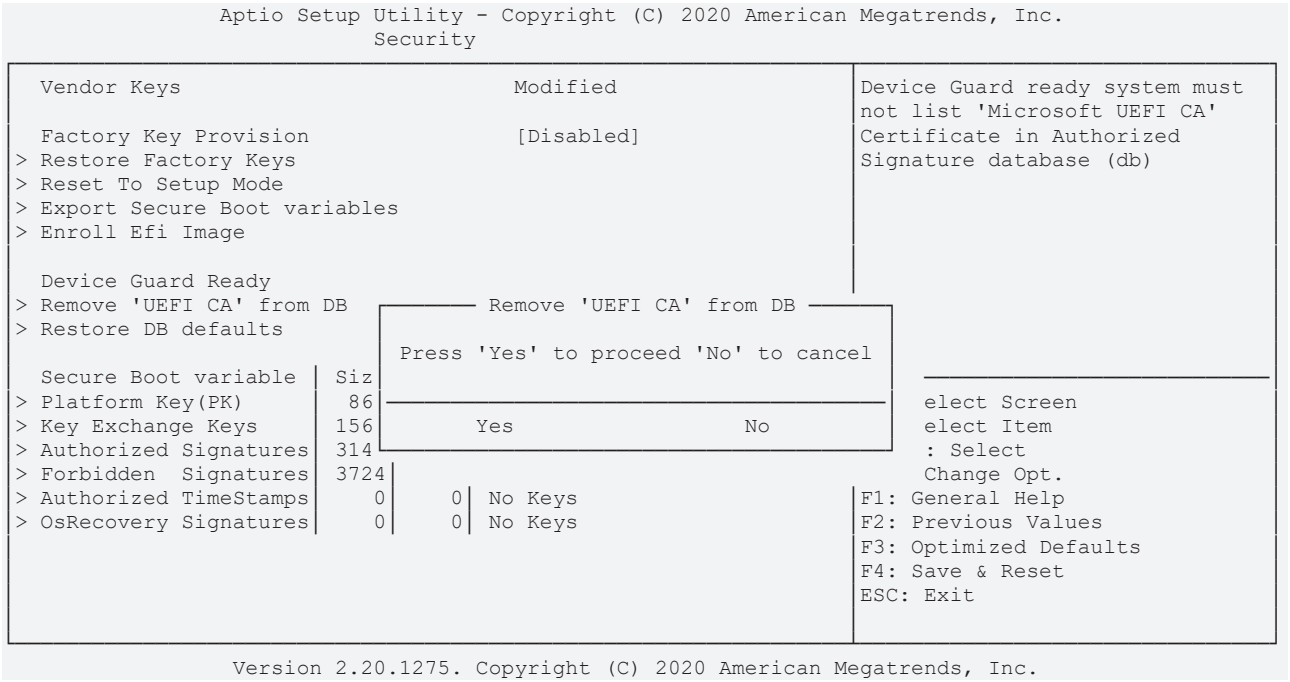
Bios entry	Options
Vendor Keys	None
Export Secure Boot variables	File system, see box

8.5.1.3.4 Enroll Efi Image



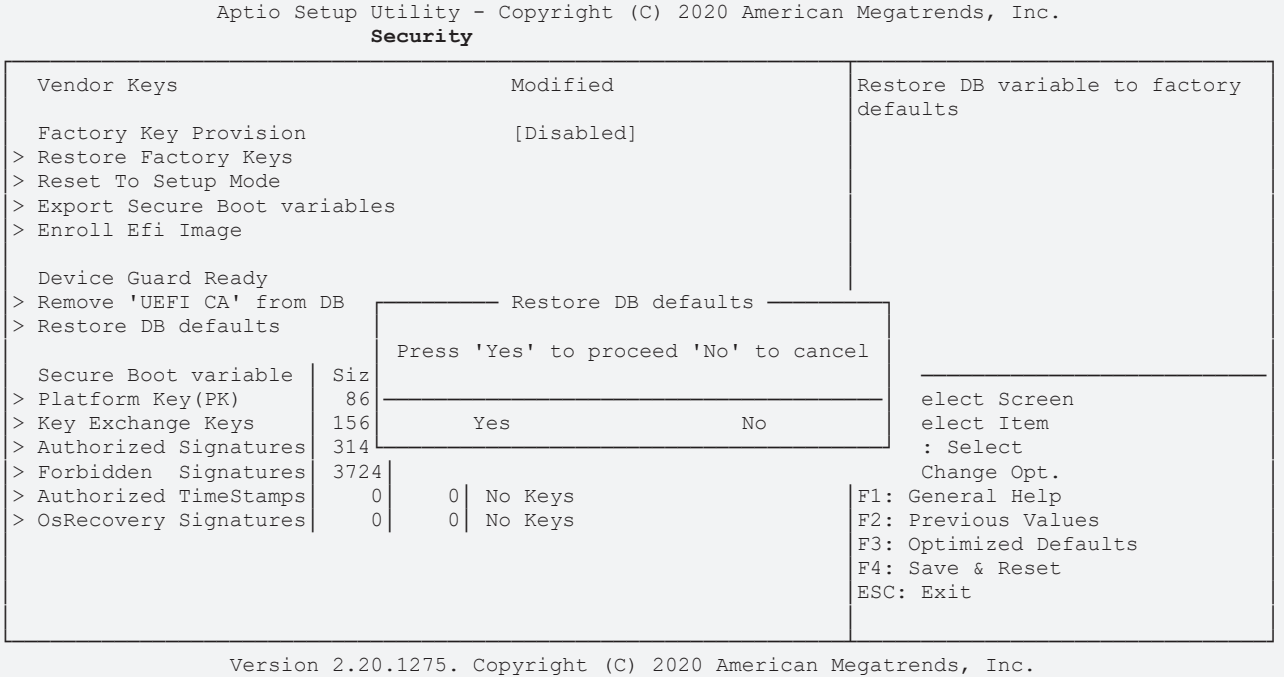
Bios entry	Options
Vendor Keys	None
Enroll Efi Image	File System, see box

8.5.1.3.5 Remove UEFI CA from DB



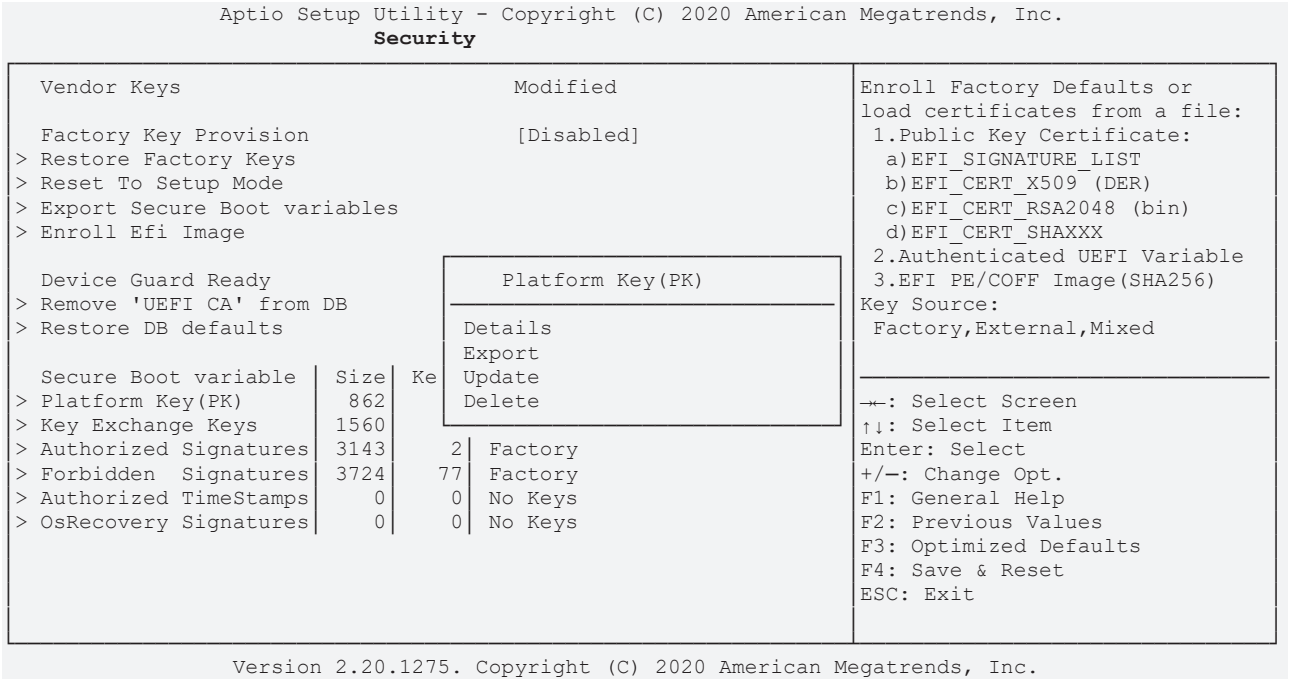
Bios entry	Options
Vendor Keys	None
Remove ‘UEFI CA’ from DB	Remove ‘UEFI CA‘ from DB, see box

8.5.1.3.6 Restore DB faults



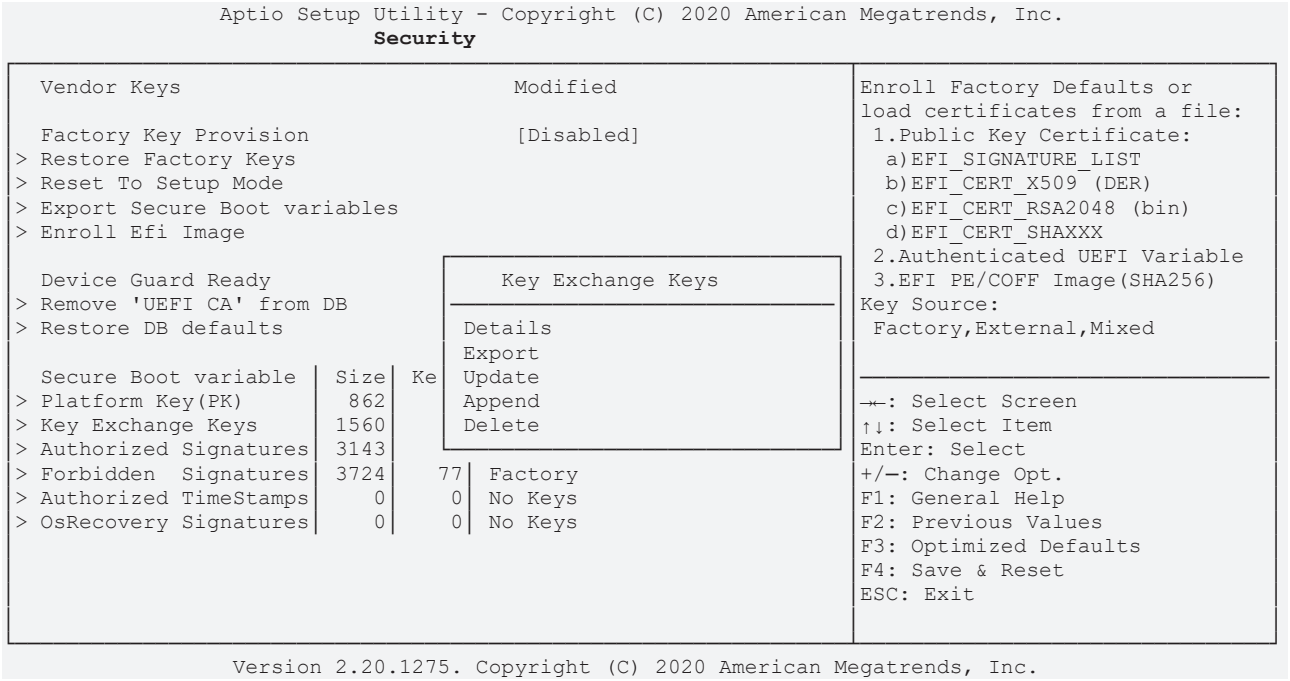
Bios entry	Options
Vendor Keys	None
Restore DB defaults	Restore DB defaults, see box

8.5.1.3.7 Platform Key (PK)



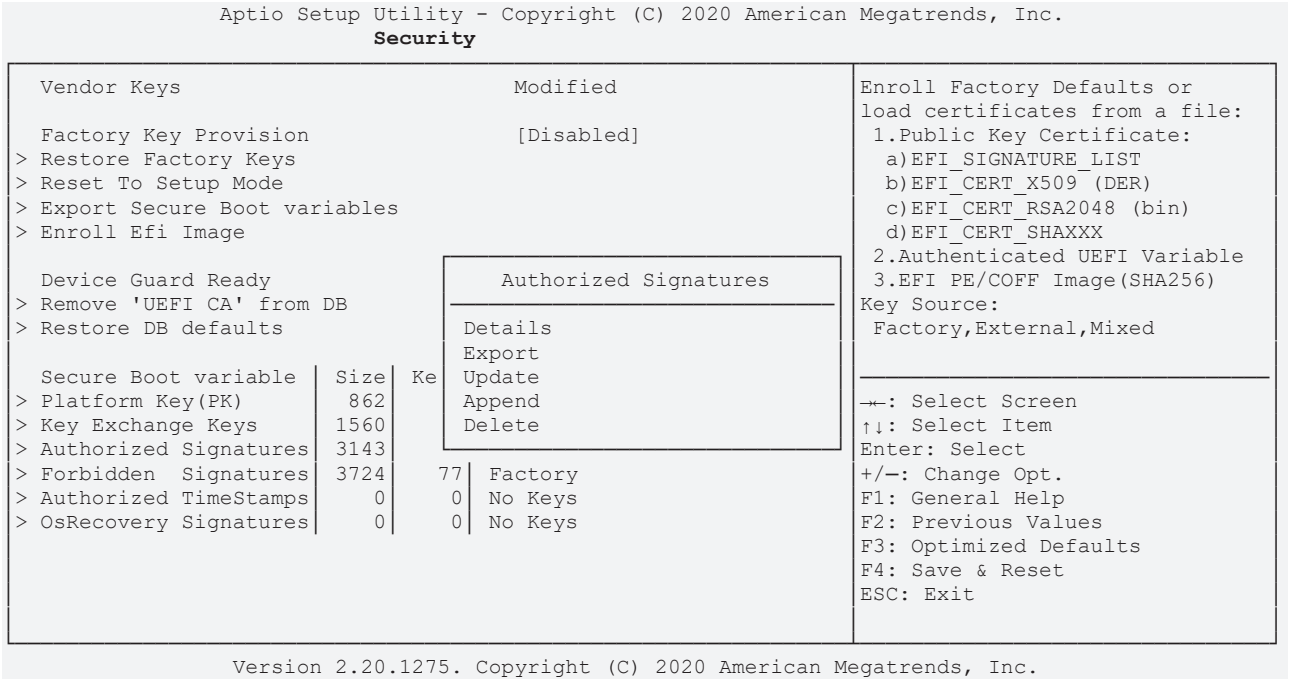
Bios entry	Options
Vendor Keys	None
Platform Key (PK)	Platform Key (PK), see box

8.5.1.3.8 Key Exchange Keys



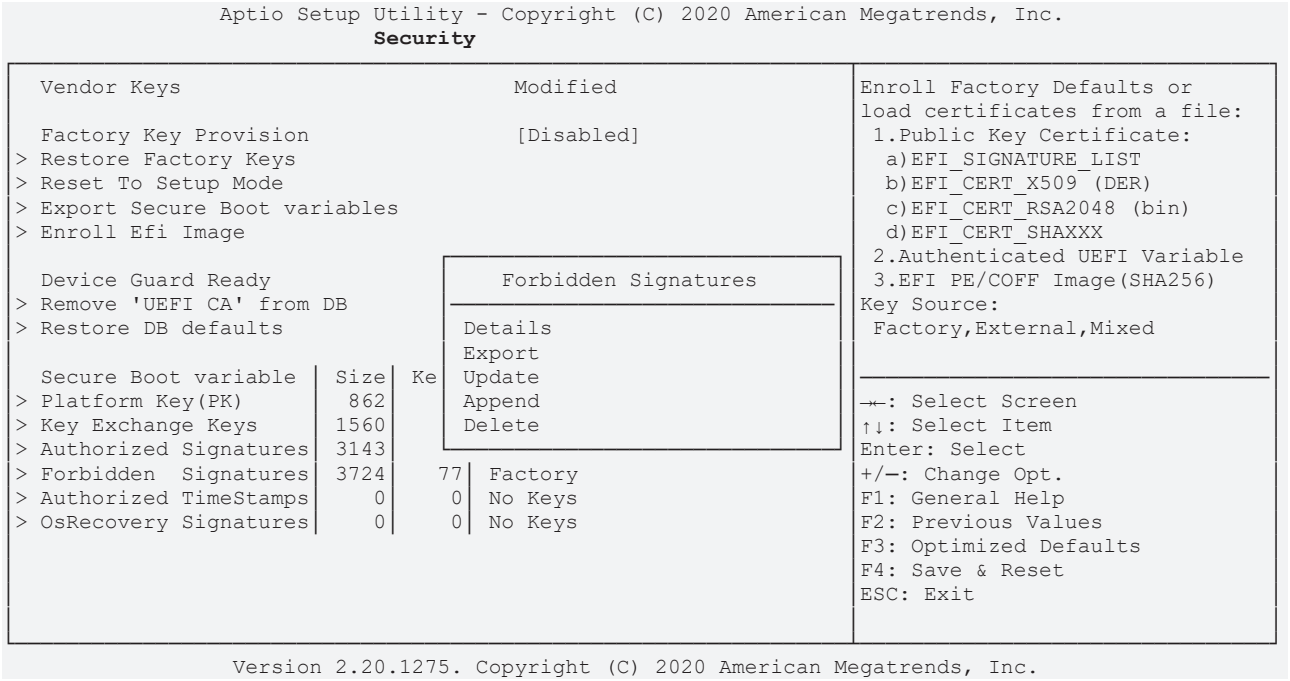
Bios entry	Options
Vendor Keys	None
Key Exchange Keys	Key Exchange Keys, see box

8.5.1.3.9 Authorized Signatures



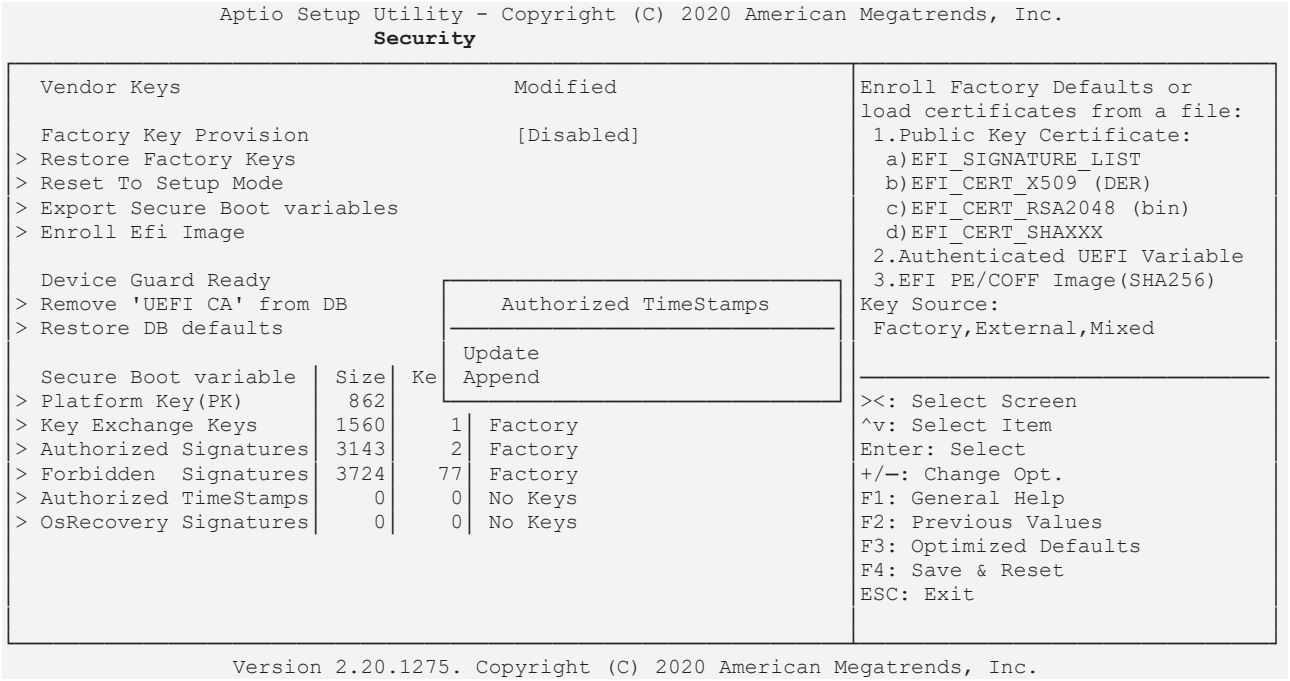
Bios entry	Options
Vendor Keys	None
Authorized Signatures	Authorized Signatures, see box

8.5.1.3.10 Forbidden Signatures



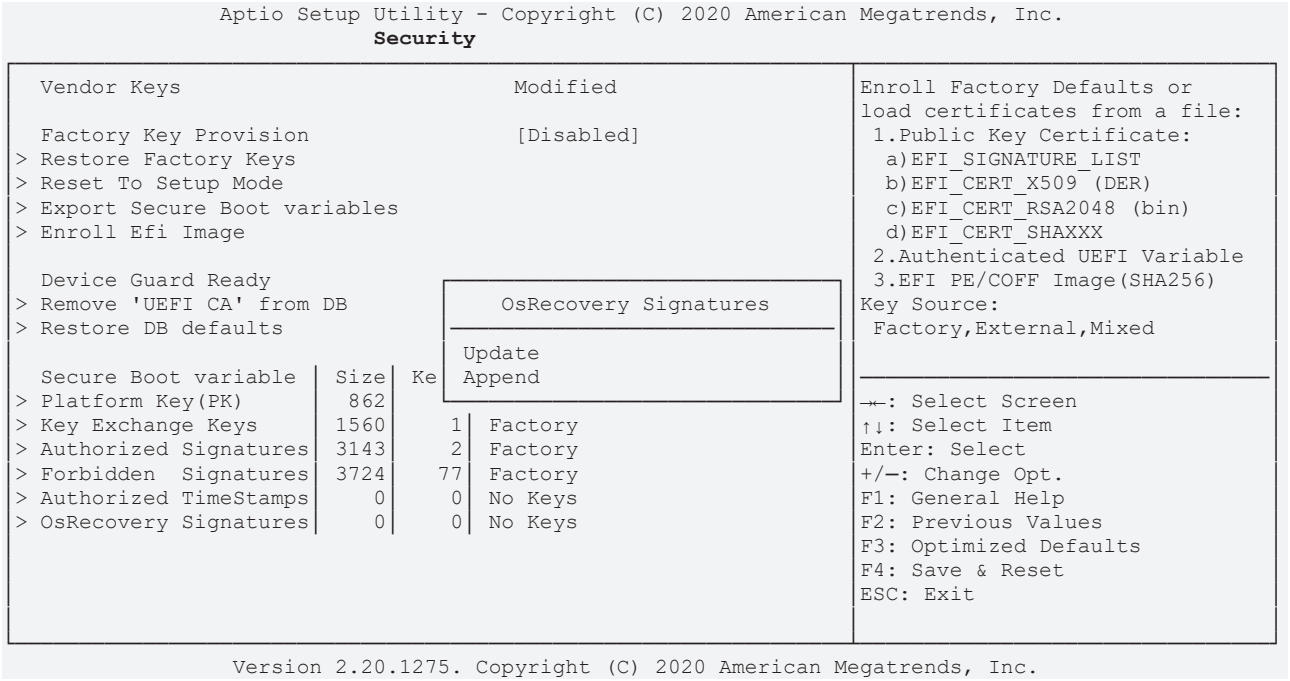
Bios entry	Options
Vendor Keys	None
Forbidden Signatures	Forbidden Signatures, see box

8.5.1.3.11 Authorized TimeStamps



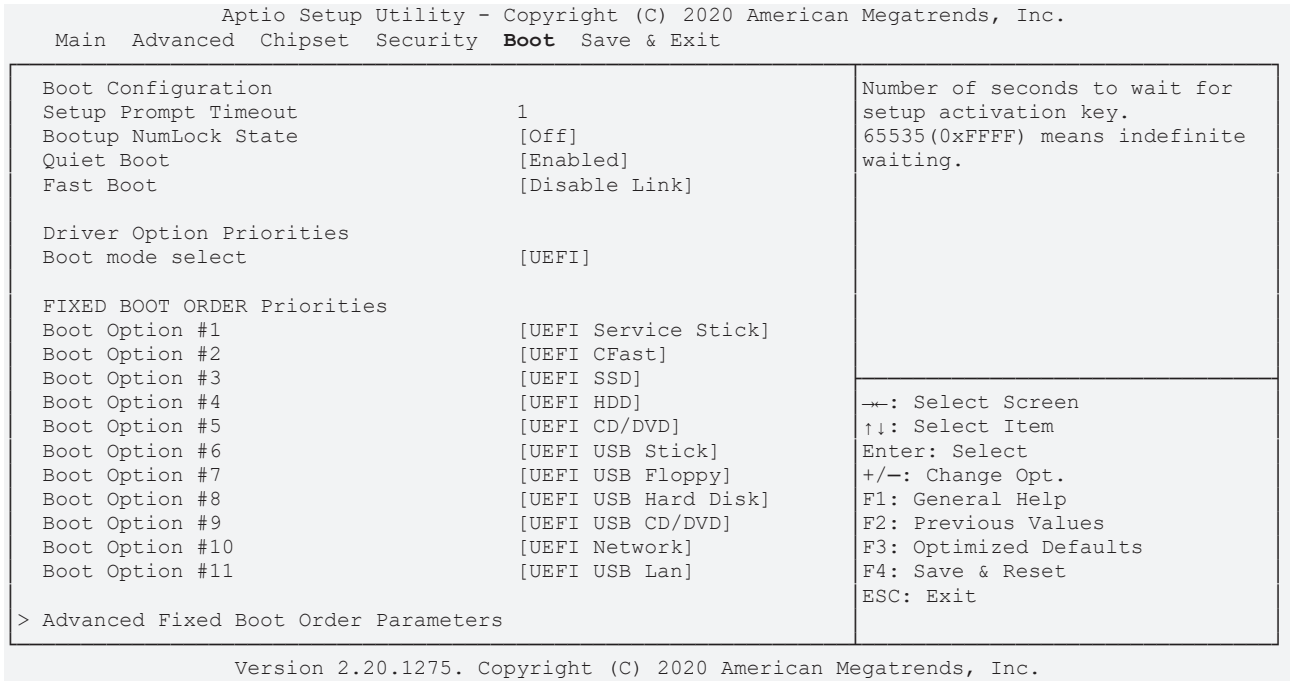
Bios entry	Options
Vendor Keys	None
Authorized TimeStamps	Authorized TimeStamps, see box

8.5.1.3.12 OsRecovery Signatures



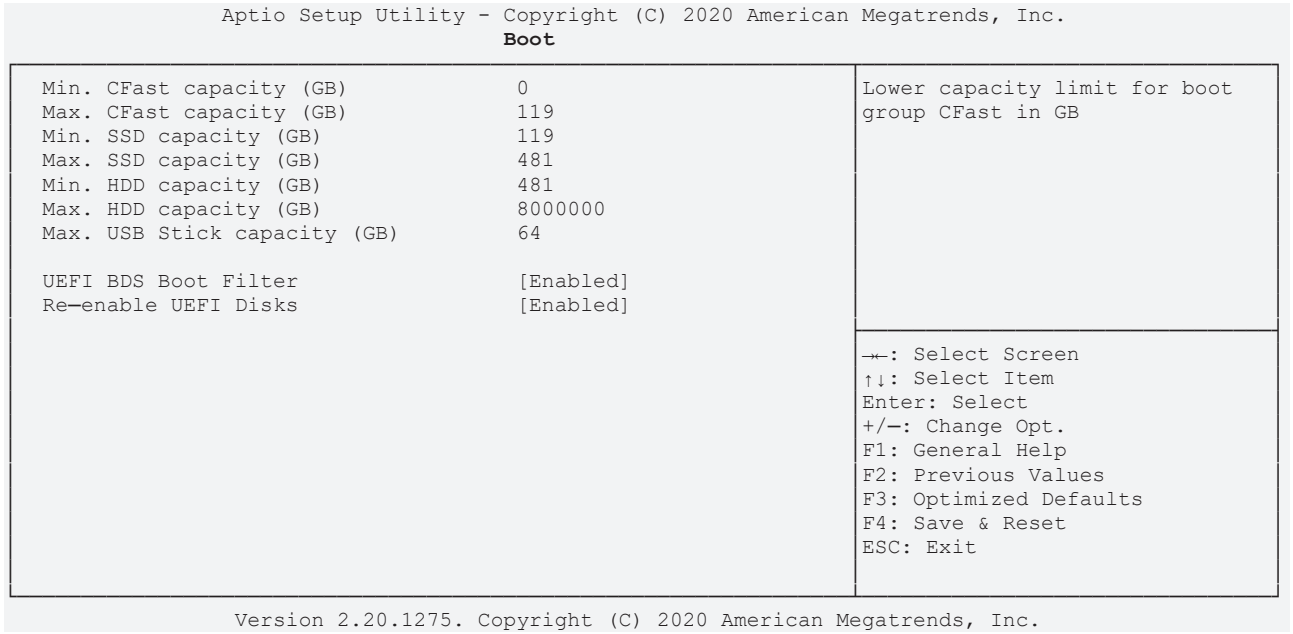
Bios entry	Options
Vendor Keys	None
OsRecovery Signatures	OsRecovery Signatures, see box

8.6 Boot



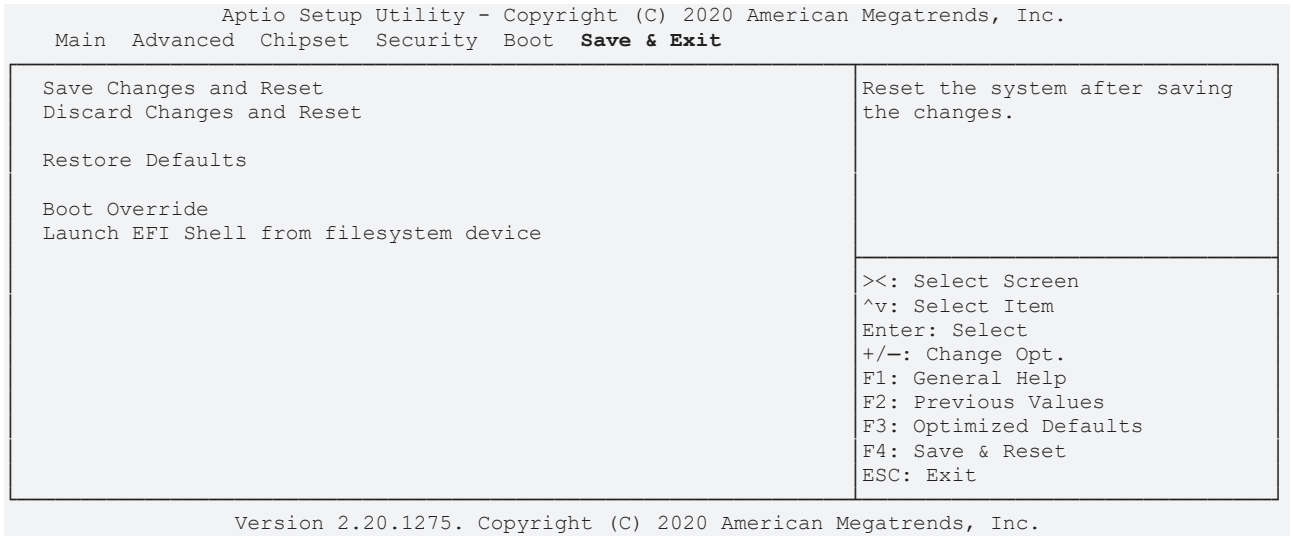
Bios entry	Options
Boot Configuration	
Setup Prompt Timeout	1
Bootup NumLok state	On/Off
Quiet Boot	Enabled/Disabled
Fast boot	Disable Link/Enabled
Driver Option Priorities	
Boot mode select	None
Fixed Boot Order Priorities	
Boot Option #1-11	Set here the order of the boot media to be used.
Advanced Fixed Boot Order Parameters	Submenu see: Fixed Boot Order Parameters [▶ 98]

8.6.1 Fixed Boot Order Parameters



Bios entry	Options
Min. CFast capacity (GB)	None
Max. CFast capacity (GB)	None
Min. SSD capacity (GB)	None
Max. SSD capacity (GB)	None
Min. HDD capacity (GB)	None
Max. HDD capacity (GB)	None
Max. USB Stick capacity (GB)	None
UEFI BDS Boot filter	Enabled/Disabled
Re-enable UEFI disks	Enabled/Disabled

8.7 Save & Exit



Bios entry	Options
Save Changes and Reset	Press enter key
Discard Changes and Reset	Press enter key
Restore Optimized Defaults	Press enter key
Boot Override	
Launch EFI Shell from filesystem device	Press enter key

8.8 BIOS update

The "DecdFlsh" program and a bootable medium with the latest BIOS version are used if the BIOS needs to be updated. When doing this it is important to start the program from a DOS environment without a virtual memory manager such as "EMM386.EXE". If such a memory manager is loaded, the program will abort with an error message or cause a crash.

DecdFlsh is a program for the automatic updating of the BIOS on all boards with AMI-BIOS. All files contained in the zip file must be unpacked into a directory, from where

```
DecdFlsh Bios-Dateiname
```

calling takes place. The name of the BIOS file and its length are checked. The BIOS will now be programmed.

The system must not be interrupted during the flashing process, as otherwise the update will abort and the BIOS on the board will be destroyed. The Flash procedure takes about 75 seconds. The necessary firmware update takes place automatically.

NOTE

Damage due to incorrect update execution

Consequences: if the BIOS update is performed incorrectly, the board can become unusable. Therefore a BIOS update should only be done if the corrections / additions that the new BIOS version brings with it are really needed.

Before a planned BIOS update, it is essential to ensure that the BIOS file to be reloaded is really released for exactly this board and for exactly this board version. If an inappropriate file is used, the board will inevitably not boot afterwards.

9 Mechanical drawing

NOTE

Dimensional notation

All dimensions in mil (1 mil = 0.0254 mm). Data in square brackets are in mm.

9.1 PCB: Outlines

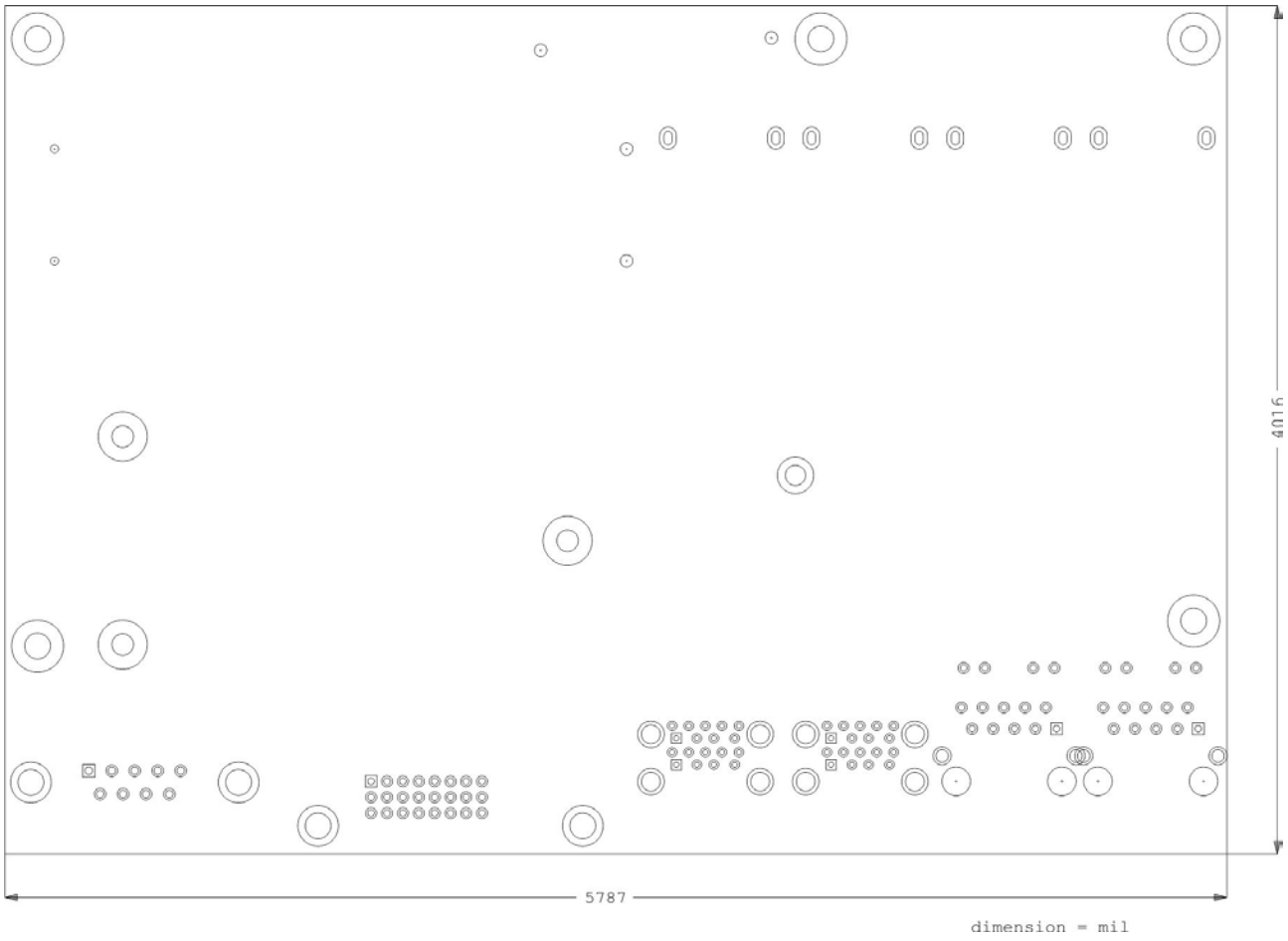


Fig. 18: CB3067-MZ

9.2 PCB: Holes

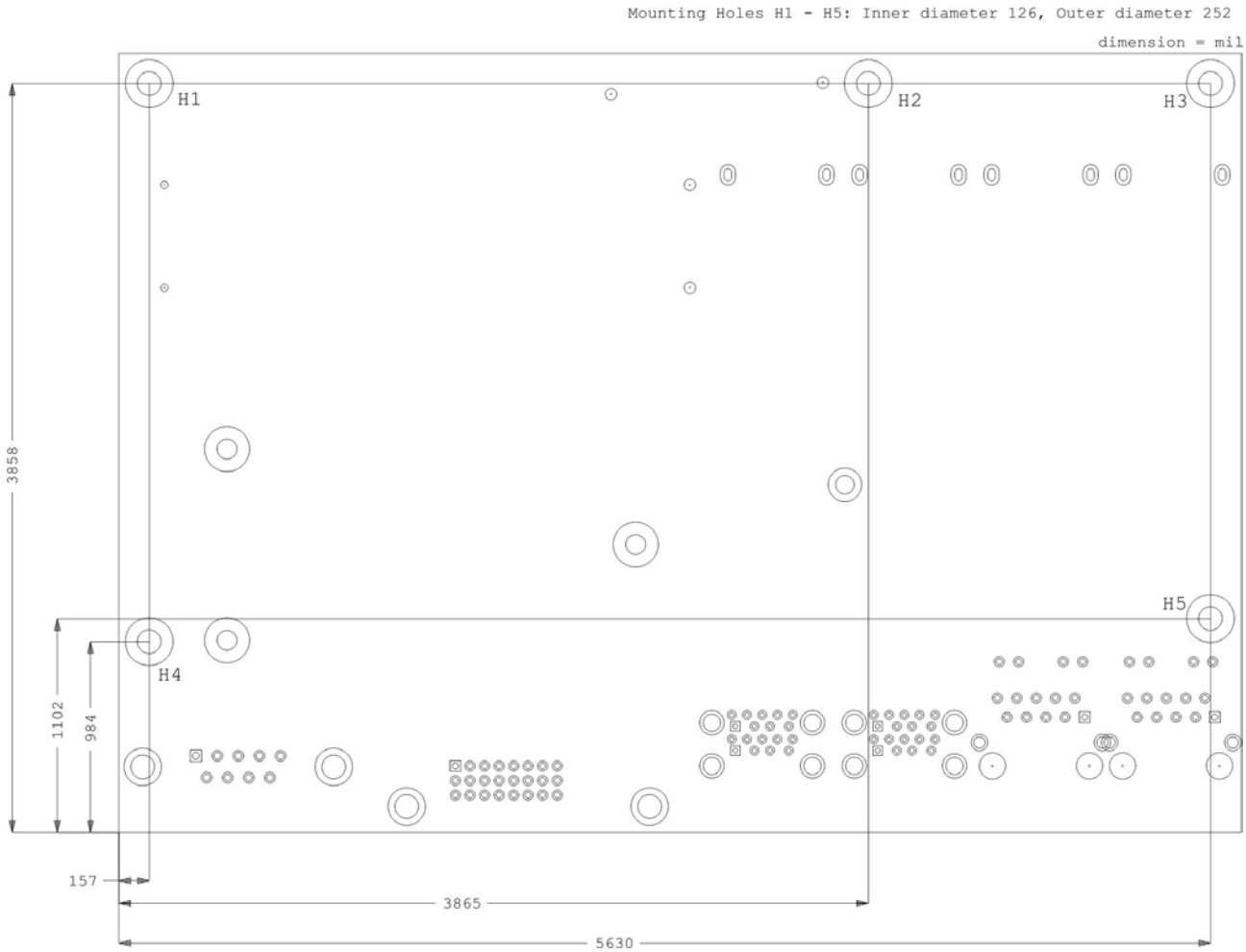


Fig. 19: CB3067-MZ-MH

9.3 PCB: Pin 1 distances

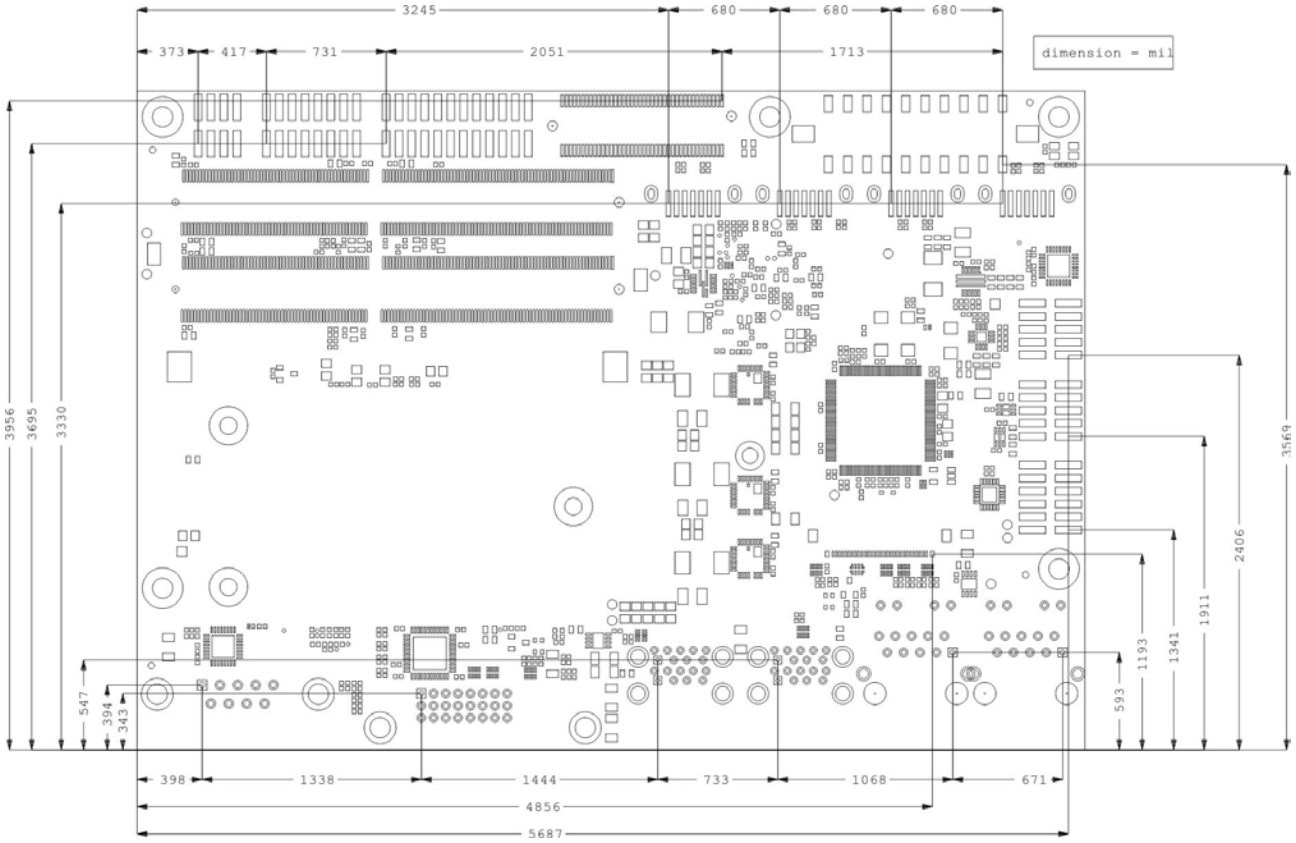


Fig. 20: CB3067-MZ-Pin1

9.4 PCB: Heat Sink

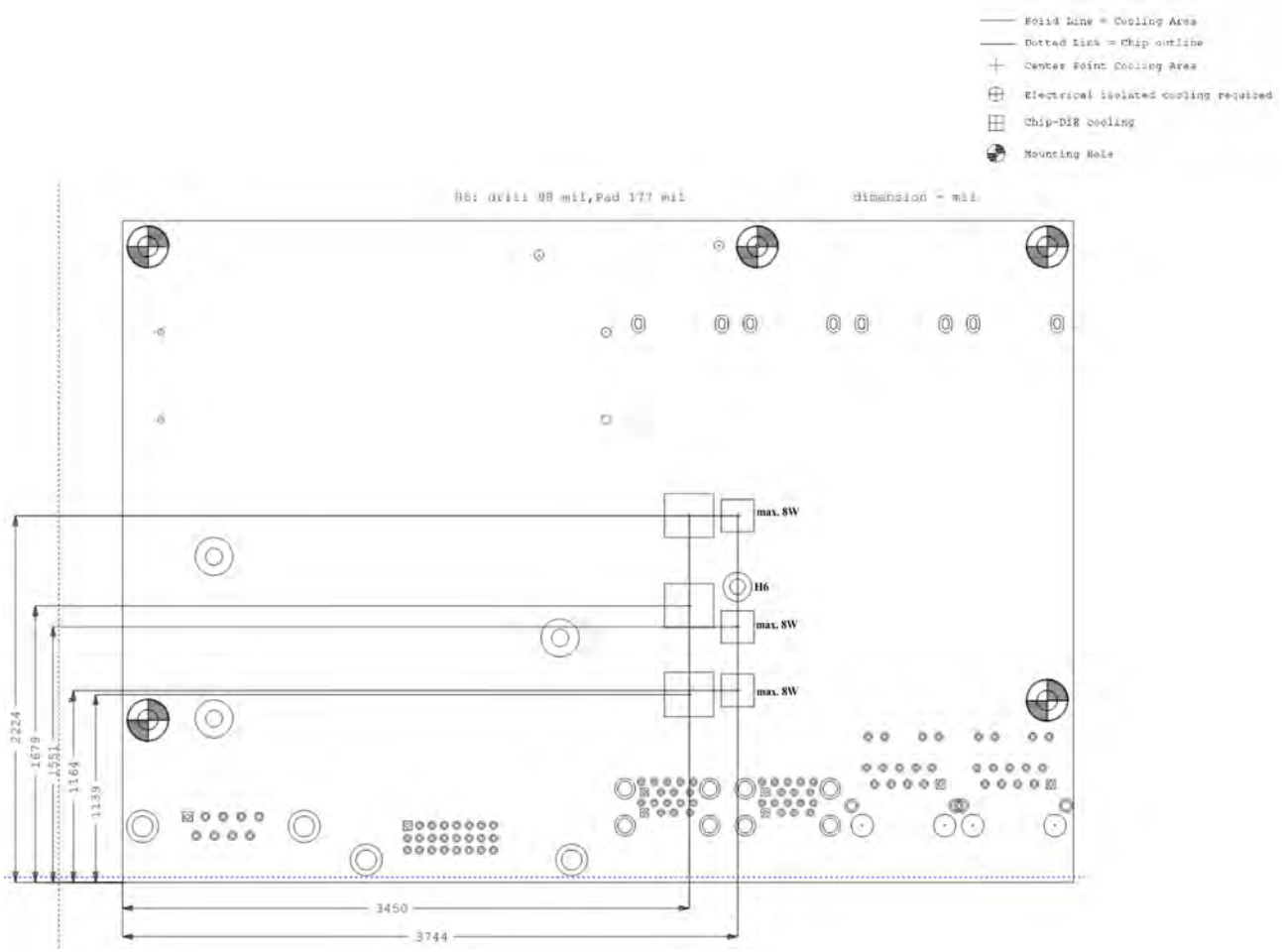


Fig. 21: CB3067-Cooling Top

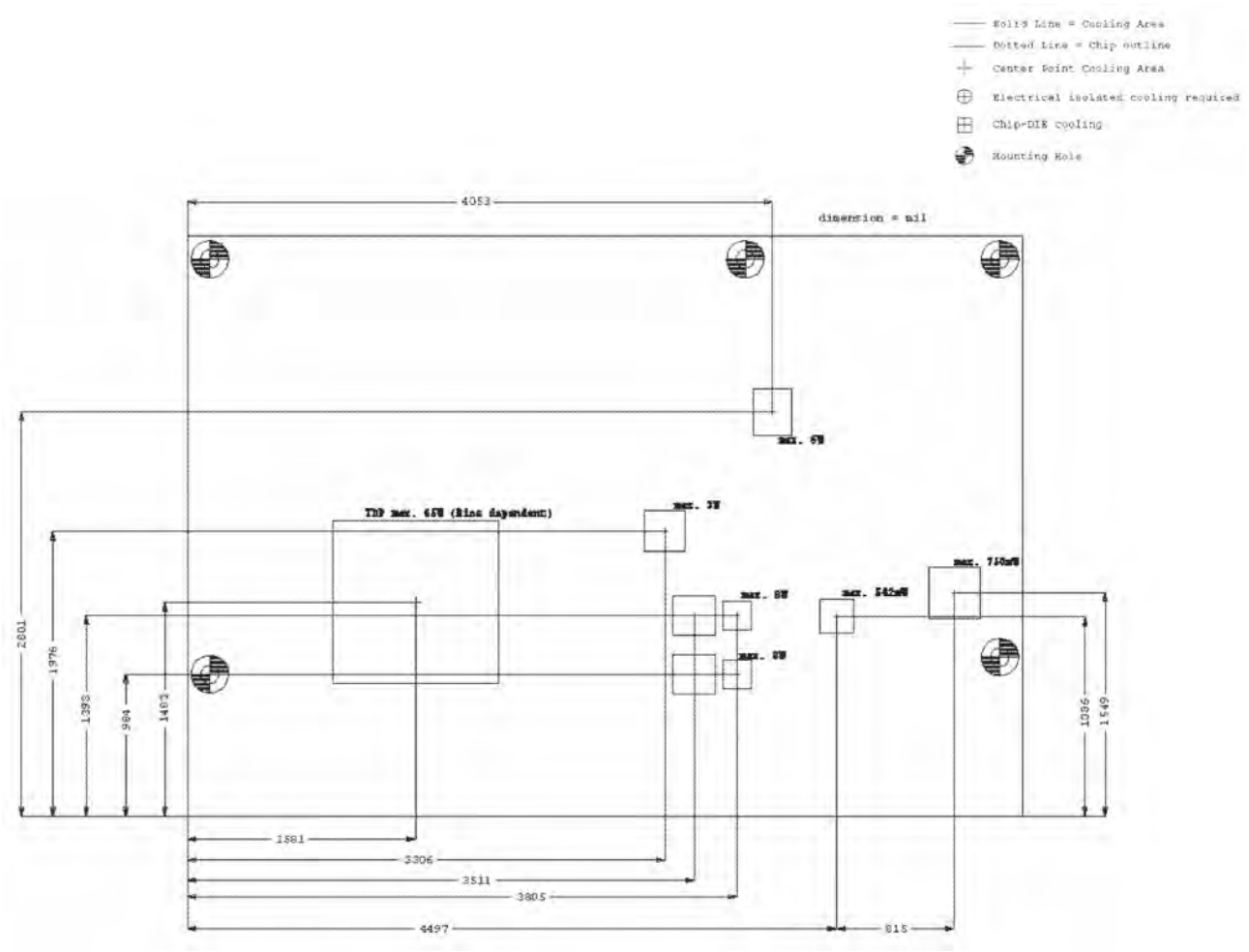


Fig. 22: CB3067-Cooling Bottom

10 Technical data

10.1 Electrical data

Power supply	
Board	5 and 12 Volt (+/- 5%)
RTC	>=3 Volt

Current consumption	
RTC	<= 10 µA

10.2 Environmental conditions

Temperature range	
Operating	0 °C to +60 °C (extended temperature range on request)
Storage	-25 °C to +85 °C
Shipping	-25 °C to +85 °C, for packed boards

Temperature changes	
Operating	0.5 °C per minute, 7.5 °C in 30 minutes
Storage	1.0 °C per minute
Shipping	1.0 °C per minute, for packed boards

Relative humidity	
Operating	5% to 85% (non-condensing)
Storage	5% to 95% (non-condensing)
Shipping	5% to 100% (non-condensing), for packed boards

Impact	
Operating	150 m/s², 6 ms
Storage	400 m/s², 6 ms
Shipping	400 m/s², 6 ms, for packed boards

Vibration	
Operating	10 to 58 Hz, amplitude 0.075 mm
Storage	5 to 9 Hz, amplitude 3.5 mm 9 to 500 Hz, 10 m/s²
Shipping	5 to 9 Hz, amplitude 3.5 mm 9 to 500 Hz, 10 m/s², for packed boards

Note on impact and vibration resistance

The specifications for impact and vibration resistance refer only to the motherboard itself without heat sink, memory module, cabling, etc.

10.3 Thermal specifications

The board is specified for an ambient temperature range from 0°C to +60°C (extended temperature range on request). In addition, care must be taken that the temperature of the processor die does not exceed 100 °C. To ensure this a suitable cooling concept must be implemented that is oriented to the maximum power consumption of the processor/chipset. It must also be ensured that any existing controllers are included in the cooling concept. The power consumption of these function blocks may be of the same order of magnitude as the power consumption of the processor.

The board is prepared with drill holes for the use of suitable cooling solutions. We have a series of compatible cooling components in our range. Your distributor will be pleased to assist you in selecting suitable solutions.

NOTE

Prevent the maximum die temperature being exceeded!

It is the end customer's responsibility to ensure that the die temperature of the processor does not exceed 100 °C! Continuous overheating can destroy the board!

If the temperature exceeds 100 °C, the ambient temperature needs to be reduced. Ensure sufficient air circulation if necessary.

11 Support and Service

Beckhoff and their partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

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- and extensive training program for Beckhoff system components

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12 Appendix I: Post Codes

During the boot phase, the BIOS generates a series of status messages (so-called "POST Codes"), which can be output with the help of a suitable reading device (POST Code card). The meanings of the POST Codes are explained in the document "Aptio™ 5.x Status Codes" from American Megatrends®, which is available from the website http://www.ami.com. In addition, the following OEM POST Codes are output:

Code	Description
87h	BIOS-API started
88h	PCA9535 started
89h	PWRCTRL firmware started

13 Appendix II: Resources

13.1 Interrupt

The resources used are independent of the setup setting. The listed interrupts and their use are given by the AT compatibility. If interrupts are to be available only on the ISA side, they must be reserved by the BIOS setup. Exclusivity on the PCI side is neither given nor possible.

13.2 PCI devices

The PCI devices listed here all exist on the board, including those that are detected and configured by the BIOS. Due to the BIOS setup settings it may be the case that various PCI devices or functions of devices are not activated. If devices are deactivated, the bus numbers of other devices may change as a result.

Bus	Dev.	Fct.	Controller / Slot
00	00	00	Host bridge ID 3E30
00	01	00	PCI-to- PCI bridge ID1901
00	01	01	PCI-to- PCI bridge ID1905
00	01	02	PCI-to- PCI bridge ID1909
00	02	00	VGA controller ID3E98
00	08	00	System device ID1911
00	12	00	Data acquisition/signal processing controller ID A379
00	14	00	XHCI USB controller ID A36D
00	14	02	RAM controller ID A36F
00	16	00	Communication device ID A360
00	16	03	Serial device ID A363
00	17	00	RAID controller ID 2822
00	1D	00	PCI-to-PCI bridge ID A330
00	1D	04	PCI-to-PCI bridge ID A334
00	1F	02	ISA bridge ID A306
00	1F	03	HD audio device ID A348
00	1F	04	SMBus controller ID A323
00	1F	05	Controller ID A324
00	1F	06	Ethernet controller ID 15BB
01	00	00	Ethernet controller (PCIE) ID 1533
02	00	00	Ethernet controller (PCIE) ID 1533
03	00	00	Ethernet controller (PCIE) ID 1533
05	00	00	Mass Storage Controller (PCIE) ID 5008

13.3 SMB devices

The following table lists the reserved SM-Bus device addresses in 8-bit notation.

NOTE

These address ranges may not be used by external devices even if the component assigned in the table doesn't exist on the motherboard.

Address	Function
34-35	API access to power supply unit
36-39	Reserved
5C-5D	NCT7491
60-6F	Reserved for DDR4
70-73	POST Code output
88-89	Slave address defined by BIOS
A0-A7	Reserved for DDR4
B0-B3	Power controller (access via BIOS-API)
B8-BB	Power controller (access via BIOS-API)

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