Hardware Data Sheet Section II

EtherCAT® Slave Controller

Section I – Technology
(Online at http://www.beckhoff.com)

Section II – Register Description
Register overview and detailed description

Section III – Hardware Description
(Online at http://www.beckhoff.com)

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BECKHOFF

DOCUMENT ORGANIZATION

The Beckhoff EtherCAT Slave Controller (ESC) documentation covers the following Beckhoff ESCs:

- ET1200
- ET1100
- EtherCAT IP Core for Intel® FPGAs
- EtherCAT IP Core for Xilinx® FPGAs
- ESC20

The documentation is organized in three sections. Section I and section II are common for all Beckhoff ESCs, Section III is specific for each ESC variant.

The latest documentation is available at the Beckhoff homepage (http://www.beckhoff.com).

Section I – Technology (All ESCs)

Section I deals with the basic EtherCAT technology. Starting with the EtherCAT protocol itself, the frame processing inside EtherCAT slaves is described. The features and interfaces of the physical layer with its two alternatives Ethernet and EBUS are explained afterwards. Finally, the details of the functional units of an ESC like FMMU, SyncManager, Distributed Clocks, Slave Information Interface, Interrupts, Watchdogs, and so on, are described.

Since Section I is common for all Beckhoff ESCs, it might describe features which are not available in a specific ESC. Refer to the feature details overview in Section III of a specific ESC to find out which features are available.

Section II – Register Description (All ESCs)

Section II contains detailed information about all ESC registers. This section is also common for all Beckhoff ESCs, thus registers, register bits, or features are described which might not be available in a specific ESC. Refer to the register overview and to the feature details overview in Section III of a specific ESC to find out which registers and features are available.

Section III – Hardware Description (Specific ESC)

Section III is ESC specific and contains detailed information about the ESC features, implemented registers, configuration, interfaces, pinout, usage, electrical and mechanical specification, and so on. Especially the Process Data Interfaces (PDI) supported by the ESC are part of this section.

Additional Documentation

Application notes and utilities can also be found at the Beckhoff homepage. Pinout configuration tools for ET1100/ET1200 are available. Additional information on EtherCAT IP Cores with latest updates regarding design flow compatibility, FPGA device support and known issues are also available.

DOCUMENT HISTORY

Version	Comment
1.0	Initial release
1.1	• Latch0/1 state register bit 0x09AE[2] and 0x09AF[2] added (ET1100 and IP Core) • On-chip Bus configuration for Avalon®: Extended PDI configuration register 0x0152[1:0] added
1.2	• On-chip Bus configuration: Extended PDI configuration register 0x0152[1:0] now valid for both Avalon and OPB • ESC DL Status: PDI Watchdog Status constantly 1 for ESC10 • EEPROM Control/Status: Selected EEPROM Algorithm not readable for ESC10/20
1.3	• EEPROM/MII Management Interface: Added self-clearing feature of command register • SPI extended configuration (0x0152:0x0153): Reset Value is EEPROM word 3, not word 1 • ESC DL Control (0x0100[0]): Added details about Source MAC address change • Power-On Values ET1100 (0x0E000): P_CONF does not correspond with physical ports
1.4	• Sync/Latch PDI configuration register: Latch configuration clarified • AL Control register: mailbox behavior described • Editorial changes
1.5	• ESC DL Control (0x0100:0x0103): FIFO Size description enhanced • IP Core: Extended Features (reset value of User RAM 0x0F80:0x0FFF) added • MII Management Interface: Write access by PDI is only possible for ET1100 if Transparent Mode is enabled. Corrected register read/write descriptions. • MII Management Control/Status register (0x0510:0x0511): Error bit description clarified. Write Enable bit is self-clearing. • ESC DL Control (0x0100:0x0103): Temporary setting DL not available for ESC10/20 • EEPROM PDI Access State register (0x0501): write access depends on EEPROM configuration • EEPROM Control/Status register (0x0502:0x0503): Error bit description clarified. Write Enable bit is self-clearing. • Registers initialized from EEPROM have Reset value 0, and EEPROM value after EEPROM was loaded successful • AL Event Request (0x0220:0x0223) description clarified: SyncManager configuration changed interrupt indicates activation register changes. • DC Latch0/1 Status (0x09AE:0x09AF): Event flags are only available in Single event mode • DC SYNC0 Cycle Time (0x09A0:0x09A3): Value of 0 selects single pulse generation • 64 Bit Receive Time ECAT Processing Unit (0x0918:0x091F) is also available for 32 Bit DCs. Renamed register to Receive Time ECAT Processing Unit • RAM Size (0x0006) ET1200: 1 Kbyte • Editorial changes

Version	Comment
1.6	• EEPROM Control/Status register (0x0502:0x0503): Error bit description clarified • EEPROM Interface and MII Management Interface: access to special registers is blocked while interface is busy • EEPROM Interface: EEPROM emulation by PDI added • Extended IP Core features (0x0F80:0x0FFF): reset values moved to Section III • Reset values of DC Receive Time registers are undefined • MI Control/Status register bit 0x510[7] is read only • FMMUs supported (0x0004): ET1200 has 3 FMMUs, not 4 • AL Event Request register: SyncManager changed flag (0x220[4]) is not available in IP Core versions before and including 1.1.1/1.01b • Configured Station Alias (0x0012:0x0013) is only taken over at first EEPROM load after power-on or reset • Moved available PDIs depending on ESC to Section I • SyncManager PDI Control (0x807 etc.): difference between read and write access described • General Purpose I/O registers (0x0F10:0x0F1F) width variable (1/2/4/8 Byte) • MII Management Interface enhancement: link detection and assignment to PDI added • Write access to DC Time Loop Control unit by PDI configurable for IP Core (V2.0.0/2.00a) • Editorial changes
1.7	• MII Management Control/Status (0x0510) updated: PHY address offset is 5 bits, feature bits have moved • System time register (0x0910:0x0917): clarified functionality • Process Data RAM (0x1000 ff.): accessible only if EEPROM is loaded • Digital I/O extended configuration (0x0152:0x0153): Set to 0 in bidirectional mode • Editorial changes
1.8	• DC register accessibility depends on DC power saving settings in PDI Control register (0x0140[11:10]) • AL Event Request register (0x0220): AL Control Event (Bit 0) is cleared by reading AL Control register (0x0120), not AL Event Request register • EEPROM Control/Status register bit 0x0502[12] renamed to EEPROM loading status • Description of Push-Pull/Open-Drain output drivers for SPI, µController, and SYNC0/1 enhanced • Speed Counter Start register (0x0930:0x0931): Write access resets calculated Time Loop Control values • Speed Counter Diff register (0x0932:0x0933): Deviation calculation added • DC Start Time Cyclic operation (0x0990:0x0997) and Next Sync1 Pulse (0x0998:0x099F) relate to the System time • Reset DC Control loop (write 0x0930:0x0931) after changing filter depths (0x0934 or 0x0935) • Editorial changes
1.9	• Update to EtherCAT IP Core Release 2.2.0/2.02a • Register availability added • Writing to DC Filter Depth registers 0x0934:0x0935 resets filters • DC Activation register (0x0981) enhanced • DC Activation state register (0x0984) added • Reserved registers or register bits: write 0, ignore read values • Enhanced link detection 0x0141[1] has compatibility issues with EBUS ports, not MII ports • Port dependent Enhanced link detection (0x0140[15:12] added • PHY Port y Status bit 5 added (port configuration updated) • ESC10 removed • Editorial changes

Version	Comment
2.0	• DC SYNC Activation register (0x0981[6]): bit polarity corrected • Deviation calculation formula for Speed Counter Diff register (0x0932:0x0933) corrected • AL Event Mask register (0x0204:0x0207): corresponding to AL Event Request register bits, not to ECAT Event Request register bits • Register availability noted in ESC availability tabs • Register Digital I/O configuration (0x0150): corrected OUTVALID mode = 1 description • Power-on values ET1200 (0x0E00[6]): CLK25OUT on PDI[6], not PDI[31] • Editorial changes
2.1	• Register bit 0x0220[4] is not available for ESC20 • DC System Time (0x0910:0x0917): read value differs between ECAT and PDI • DC Latch Times and DC Event Times are internally latched when lowest byte is read • DC Speed Counter Start (0x0930:0x0931): minimum value is 0x80 • Editorial changes
2.2	• ESC20: Register Configured Station Alias (0x0012:0x0013) is taken over after each EEPROM reload command • MII Management Control register 0x0510[0]: Updated to ET1100-0002 • Registers 0x0020 and 0x0030 are readable for ET1100 and ET1200 • Editorial changes
2.3	• Update to EtherCAT IP Core Release 2.3.0/2.03a (registers 0x0138/0x0139, 0x0150 On-chip Bus, 0x0220, 0x030E, 0x0805 affected) • Separated registers 0x0140 (PDI Control) and 0x0141 (now: ESC Configuration) • Editorial changes
2.4	• ESC DL Control register (0x0100[0]) description changed • Added ESC Feature Bits 0x0008[11:9] • Update to EtherCAT IP Core Release 2.3.2/2.03c • ESC Features 0x0008 and ESC Configuration 0x0141[1]: Enhanced Link Detection must not be activated for ET1100/ET1200 if EBUS ports are used. • Editorial changes
2.5	• Update to EtherCAT IP Core Release 2.4.0/2.04a • ESC20: 0x0140[1:0] and [5:4] are available for SPI PDI • Range for DC Speed Counter Start (0x0930:0x0931) and Speed Counter Diff (0x0932:0x0933) corrected, representation of Speed Counter Diff mentioned.
2.6	• Update to EtherCAT IP Core Release 3.0.0 • Added Register DC Receive Time Latch Mode 0x0936 • Device Identification in AL Control/Status register 0x0120/0x0130 added • Editorial changes
2.7	• Update to EtherCAT IP Core Release 2.4.3/2.04d and 3.0.2/3.00c • Editorial changes
2.8	• Update to EtherCAT IP Core Release 3.0.10/3.00k • Clarified DC Receive Time latching • ESC DL Control register (0x0100[0]): Source MAC address bit is set depending on the forwarding rule, but not depending on the frame content. • DC System Time Difference (0x092C:0x092F) bit [31] description corrected • Read values of DC Start Time Cyclic Operation (0x0990:0x0997), Next Sync1 Pulse (0x0998:0x099F are latched when first byte is read • Corrected PDI register function acknowledge by write for SyncManager Activation register 0x0806 • Removed chapter ESC Register Availability, please refer to Application Note ESC Comparison • Editorial changes
2.9	• Altera is now Intel • Editorial changes

Version	Comment
3.0	• Update to EtherCAT IP Core Release 3.0.10/3.00k Patch3 • Clarified Distributed Clocks Start Time Cyclic Operation (0x0990:0x0997) extension and auto-activation • Enhanced PDI Error Code register 0x030E to 0x030E:0x030F • Added Avalon and AXI PDI Error Code 0x030E:0x030F • Enhanced ESC Reset ECAT/PDI 0x0040:0x0041 description • Editorial changes

CONTENTS

TABLES

ABBREVIATIONS

ADR	Address
AL	Application Layer
APRW	Auto Increment Physical ReadWrite
BHE	Bus High Enable
BWR	Broadcast Write
DC	Distributed Clock
DL	Data Link Layer
ECAT	EtherCAT
ESC	EtherCAT Slave Controller
ESI	EtherCAT Slave Information
FCS	Frame Check Sequence
FMMU	Fieldbus Memory Management Unit
FPRD	Configured Address Physical Read
FPRW	Configured Address Physical ReadWrite
FPWR	Configured Address Physical Write
GPI	General Purpose Input
GPO	General Purpose Output
IP	Intellectual Property
µC	Microcontroller
MI	(PHY) Management Interface
MII	Media Independent Interface
OPB	On-Chip Peripheral Bus
PDI	Process Data Interface
RMII	Reduced Media Independent Interface
SII	Slave Information Interface
SM	SyncManager
SoC	System on a Chip
SOF	Start of Frame
SoPC	System on a Programmable Chip
SPI	Serial Peripheral Interface
WD	Watchdog

1 Address Space Overview

An EtherCAT Slave Controller (ESC) has an address space of 64KByte. The first block of 4KByte (0x0000:0x0FFF) is dedicated to registers. The Process Data RAM starts at address 0x1000, its size depends on the ESC. The availability of the registers depends on the ESC.

Table 1: ESC address space

Address[1]	Length (Byte)	Description
		ESC Information
0x0000	1	Type
0x0001	1	Revision
0x0002:0x0003	2	Build
0x0004	1	FMMUs supported
0x0005	1	SyncManagers supported
0x0006	1	RAM Size
0x0007	1	Port Descriptor
0x0008:0x0009	2	ESC Features supported
		Station Address
0x0010:0x0011	2	Configured Station Address
0x0012:0x0013	2	Configured Station Alias
		Write Protection
0x0020	1	Register Write Enable
0x0021	1	Register Write Protection
0x0030	1	ESC Write Enable
0x0031	1	ESC Write Protection
		Data Link Layer
0x0040	1	ESC Reset ECAT
0x0041	1	ESC Reset PDI
0x0100:0x0103	4	ESC DL Control
0x0108:0x0109	2	Physical Read/Write Offset
0x0110:0x0111	2	ESC DL Status
		Application Layer
0x0120:0x0121	2	AL Control
0x0130:0x0131	2	AL Status
0x0134:0x0135	2	AL Status Code
0x0138	1	RUN LED Override
0x0139	1	ERR LED Override
		PDI / ESC Configuration
0x0140	1	PDI Control
0x0141	1	ESC Configuration
0x014E:0x014F	2	PDI Information
0x0150	1	PDI Configuration
0x0151	1	SYNC/LATCH[1:0] PDI Configuration
0x0152:0x0153	2	Extended PDI Configuration

[1] Address areas not listed here are reserved. They are not writable. Read data from reserved addresses has to be ignored. Reserved addresses must not be written.

Address[1]	Length (Byte)	Description
		Interrupts
0x0200:0x0201	2	ECAT Event Mask
0x0204:0x0207	4	PDI AL Event Mask
0x0210:0x0211	2	ECAT Event Request
0x0220:0x0223	4	AL Event Request
		Error Counters
0x0300:0x0307	4x2	Rx Error Counter[3:0]
0x0308:0x030B	4x1	Forwarded Rx Error counter[3:0]
0x030C	1	ECAT Processing Unit Error Counter
0x030D	1	PDI Error Counter
0x030E:0x030F	2	PDI Error Code
0x0310:0x0313	4x1	Lost Link Counter[3:0]
		Watchdogs
0x0400:0x0401	2	Watchdog Divider
0x0410:0x0411	2	Watchdog Time PDI
0x0420:0x0421	2	Watchdog Time Process Data
0x0440:0x0441	2	Watchdog Status Process Data
0x0442	1	Watchdog Counter Process Data
0x0443	1	Watchdog Counter PDI
		SII EEPROM Interface
0x0500	1	EEPROM Configuration
0x0501	1	EEPROM PDI Access State
0x0502:0x0503	2	EEPROM Control/Status
0x0504:0x0507	4	EEPROM Address
0x0508:0x050F	4/8	EEPROM Data
		MII Management Interface
0x0510:0x0511	2	MII Management Control/Status
0x0512	1	PHY Address
0x0513	1	PHY Register Address
0x0514:0x0515	2	PHY Data
0x0516	1	MII Management ECAT Access State
0x0517	1	MII Management PDI Access State
0x0518:0x051B	4	PHY Port Status
0x0600:0x06FF	**16x16**	**FMMU[15:0]**
+0x0:0x3	4	Logical Start Address
+0x4:0x5	2	Length
+0x6	1	Logical Start bit
+0x7	1	Logical Stop bit
+0x8:0x9	2	Physical Start Address
+0xA	1	Physical Start bit
+0xB	1	Type
+0xC	1	Activate
+0xD:0xF	3	Reserved

Address[1]	Length (Byte)	Description
0x0800:0x087F	**16x8**	**SyncManager[15:0]**
+0x0:0x1	2	Physical Start Address
+0x2:0x3	2	Length
+0x4	1	Control Register
+0x5	1	Status Register
+0x6	1	Activate
+0x7	1	PDI Control
0x0900:0x09FF		**Distributed Clocks (DC)**
		DC – Receive Times
0x0900:0x0903	4	Receive Time Port 0
0x0904:0x0907	4	Receive Time Port 1
0x0908:0x090B	4	Receive Time Port 2
0x090C:0x090F	4	Receive Time Port 3
		DC – Time Loop Control Unit
0x0910:0x0917	4/8	System Time
0x0918:0x091F	4/8	Receive Time ECAT Processing Unit
0x0920:0x0927	4/8	System Time Offset
0x0928:0x092B	4	System Time Delay
0x092C:0x092F	4	System Time Difference
0x0930:0x0931	2	Speed Counter Start
0x0932:0x0933	2	Speed Counter Diff
0x0934	1	System Time Difference Filter Depth
0x0935	1	Speed Counter Filter Depth
0x0936	1	Receive Time Latch Mode
		DC – Cyclic Unit Control
0x0980	1	Cyclic Unit Control
		DC – SYNC Out Unit
0x0981	1	Activation
0x0982:0x0983	2	Pulse Length of SyncSignals
0x0984	1	Activation Status
0x098E	1	SYNC0 Status
0x098F	1	SYNC1 Status
0x0990:0x0997	4/8	Start Time Cyclic Operation/Next SYNC0 Pulse
0x0998:0x099F	4/8	Next SYNC1 Pulse
0x09A0:0x09A3	4	SYNC0 Cycle Time
0x09A4:0x09A7	4	SYNC1 Cycle Time
		DC – Latch In Unit
0x09A8	1	Latch0 Control
0x09A9	1	Latch1 Control
0x09AE	1	Latch0 Status
0x09AF	1	Latch1 Status
0x09B0:0x09B7	4/8	Latch0 Time Positive Edge
0x09B8:0x09BF	4/8	Latch0 Time Negative Edge
0x09C0:0x09C7	4/8	Latch1 Time Positive Edge
0x09C8:0x09CF	4/8	Latch1 Time Negative Edge

Address[1]	Length (Byte)	Description
		DC – SyncManager Event Times
0x09F0:0x09F3	4	EtherCAT Buffer Change Event Time
0x09F8:0x09FB	4	PDI Buffer Start Event Time
0x09FC:0x09FF	4	PDI Buffer Change Event Time
		ESC specific
0x0E00:0x0EFF	256	ESC specific registers: ET1100, ET1200, (Power-On Values) IP Core (Product and Vendor ID) ESC20 (FPGA Update)
		ESC specific I/O
0x0F00:0x0F03	4	Digital I/O Output Data
0x0F10:0x0F17	1-8	General Purpose Outputs
0x0F18:0x0F1F	1-8	General Purpose Inputs
		User RAM/Extended ESC features
0x0F80:0x0FFF	128	User RAM
		Process Data RAM
0x1000:0x1003	4	Digital I/O Input Data
0x1000:0x13FF 0x1000:0x17FF 0x1000:0x1FFF 0x1000:0x2FFF 0x1000:0x4FFF 0x1000:0x8FFF 0x1000:0xFFFF	1 KB 2 KB 4 KB 8 KB 16 KB 32 KB 60 KB	Process Data RAM

For registers longer than one byte, the LSB has the lowest and MSB the highest address.

1.1 Scope of Section II

Section II contains detailed information about all ESC registers. This section is also common for all Beckhoff ESCs, thus registers, register bits, or features are described which might not be available in a specific ESC. Refer to the register overview in Section III of a specific ESC to find out which registers are available. Additionally, refer to the feature details overview in Section III of a specific ESC to find out which features are available.

The following Beckhoff ESCs are covered by Section II:

- ET1200-0003
- ET1100-0003
- EtherCAT IP Core for Intel FPGAs (V2.4.4 / V3.0.10 Patch 3)
- EtherCAT IP Core for Xilinx FPGAs (V2.04e / V3.00k Patch 3)
- ESC20 (Build 22)

1.2 Reserved Registers/Reserved Register Bits

Reserved registers must not be written, reserved register bits have to be written as 0. Read values of reserved registers or register bits have to be ignored. Reserved registers or register bits initialized by EEPROM values have to be initialized with 0.

Reserved EEPROM words of the ESC configuration area have to be 0.

1.3 ESC Availability Tab Legend

The availability of registers and exceptions for individual register bits or IP Core versions are indicated in a small area at the top right edge of each register table.

Example 1:

~~ESC20~~	**ET1100**	**ET1200**	**IP Core**
		~~[5]~~	V2.0.0/ V2.00a

- Register is not available for ESC20 (reserved)
- Register is available for ET1100 (all bits mentioned below)
- Register is available for ET1200, except for bit 5 which is reserved
- Register is available for IP Core since V2.0.0/V2.00a, reserved for previous versions

Example 2:

~~ESC20~~	**ET1100**	~~ET1200~~	**IP Core**
	write config.		[5] V2.0.0/ V2.00a

- Register is available for ET1100 (read), write access is optionally available (e.g. ESI EEPROM or IP Core configuration)
- Register is available for IP Core, bit 5 is available since V2.0.0/V2.00a, bit 5 is not available for previous versions (and reserved)

Example 3:

~~ESC20~~	**ET1100**	~~ET1200~~	IP Core
	[63:16] config.		V2.0.0/ V2.00a

- Register is available for ET1100, bits [63:16] are optionally available (e.g. ESI EEPROM or IP Core configuration)
- Register is optionally available/configurable for IP Core since V2.0.0/V2.00a (“IP Core” is not **bold**)

2 Register description

2.1 Type (0x0000)

Table 2: Register Type (0x0000)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
7:0	Type of EtherCAT controller	r/-	r/-	Beckhoff: First terminals: 0x01 ESC10, ESC20: 0x02 First EK1100: 0x03 IP Core: 0x04 Internal FPGA: 0x05 ET1100: 0x11 ET1200: 0x12	

2.2 Revision (0x0001)

Table 3: Register Revision (0x0001)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
7:0	Revision of EtherCAT controller. IP Core: major version X (version X.Y.Z)	r/-	r/-	ESC dep.	

2.3 Build (0x0002:0x0003)

Table 4: Register Build (0x0002:0x0003)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
15:0	Build of EtherCAT controller. EtherCAT IP Core (version X.Y.Z): [3:0] maintenance version Z [7:4] minor version Y [15:8] patch level / development build: 0x00: original release 0x01-0x0F: patch level of original release 0x10-0xFF: development build	r/-	r/-	ESC dep.	

2.4 FMMUs supported (0x0004)

Table 5: Register FMMUs supported (0x0004)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
7:0	Number of supported FMMU channels (or entities)	r/-	r/-	ESC20: 4 IP Core: depends on configuration ET1100: 8 ET1200: 3	

2.5 SyncManagers supported (0x0005)

Table 6: Register SyncManagers supported (0x0005)

			ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**		
7:0	Number of supported SyncManager channels (or entities)	r/-	r/-	ESC20: 4 IP Core: depends on configuration ET1100: 8 ET1200: 4		

2.6 RAM Size (0x0006)

Table 7: Register RAM Size (0x0006)

			ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**		
7:0	Process Data RAM size supported in Kbyte	r/-	r/-	ESC20: 4 IP Core 0-60, depends on configuration ET1100: 8 ET1200: 1		

2.7 Port Descriptor (0x0007)

Table 8: Register Port Descriptor (0x0007)

			~~ESC20~~	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**		
	Port configuration: 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII / RMII / RGMII					
1:0	Port 0	r/-	r/-	ESC and ESC configuration dep.		
3:2	Port 1	r/-	r/-			
5:4	Port 2	r/-	r/-			
7:6	Port 3	r/-	r/-			

2.8 ESC Features supported (0x0008:0x0009)

Table 9: Register ESC Features supported (0x0008:0x0009)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
0	FMMU Operation: 0: Bit-oriented 1: Byte-oriented	r/-	r/-	0	
1	Unused register access: 0: allowed 1: not supported	r/-	r/-	0	
2	Distributed Clocks: 0: Not available 1: Available	r/-	r/-	ESC20: 1 IP Core: depends on configuration ET1100: 1 ET1200: 1	
3	Distributed Clocks (width): 0: 32 bit 1: 64 bit	r/-	r/-	ET1100: 1 ET1200: 1 IP Core: depends on configuration Others : 0	
4	Low Jitter EBUS: 0: Not available, standard jitter 1: Available, jitter minimized	r/-	r/-	ET1100: 1 ET1200: 1 Others : 0	
5	Enhanced Link Detection EBUS: 0: Not available 1: Available	r/-	r/-	ET1100: 1 ET1200: 1 Others : 0	
6	Enhanced Link Detection MII: 0: Not available 1: Available	r/-	r/-	ET1100: 1 ET1200: 1 Others : 0	
7	Separate Handling of FCS Errors: 0: Not supported 1: Supported, frames with wrong FCS and additional nibble will be counted separately in Forwarded RX Error Counter	r/-	r/-	IP Core: 1 ET1100: 1 ET1200: 1 Others : 0	
8	Enhanced DC SYNC Activation: 0: Not available 1: Available NOTE: This feature refers to registers 0x981[7:3] and 0x0984	r/-	r/-	IP Core: depends on version Others : 0	
9	EtherCAT LRW command support: 0: Supported 1: Not supported	r/-	r/-	0	
10	EtherCAT read/write command support (BRW, APRW, FPRW): 0: Supported 1: Not supported	r/-	r/-	0	
11	Fixed FMMU/SyncManager configuration: 0: Variable configuration 1: Fixed configuration (refer to documentation of supporting ESCs)	r/-	r/-	0	
15:14	Reserved	r/-	r/-	0	

2.9 Configured Station Address (0x0010:0x0011)

Table 10: Register Configured Station Address (0x0010:0x0011)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	Address used for node addressing (FPRD/FPWR/FPRW/FRMW commands).	r/w	r/-	0

2.10 Configured Station Alias (0x0012:0x0013)

Table 11: Register Configured Station Alias (0x0012:0x0013)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	Alias Address used for node addressing (FPRD/FPWR/FPRW/FRMW commands). The use of this alias is activated by Register DL Control Bit 0x0100[24]. NOTE: EEPROM value is only transferred into this register at first EEPROM load after power-on or reset. ESC20 exception: EEPROM value is transferred into this register after each EEPROM reload command.	r/-	r/w	0 until first EEPROM load, then EEPROM word 4

2.11 Register Write Enable (0x0020)

Table 12: Register Register Write Enable (0x0020)

ESC20	ET1100	ET1200	IP Core
~~read~~			read: V2.4.0/ V2.04a

Bit	Description	ECAT	PDI	Reset Value
0	If register write protection is enabled, this register has to be written in the same Ethernet frame (value does not matter) before other writes to this station are allowed. This bit is self-clearing at the beginning of the next frame (SOF), or if Register Write Protection is disabled.	r/w	r/-	0
7:1	Reserved, write 0	r/-	r/-	0

2.12 Register Write Protection (0x0021)

Table 13: Register Register Write Protection (0x0021)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	Register write protection: 0: Protection disabled 1: Protection enabled Registers 0x0000:0x0F7F are write-protected, except for 0x0020 and 0x0030.	r/w	r/-	0
7:1	Reserved, write 0	r/-	r/-	0

2.13 ESC Write Enable (0x0030)

Table 14: Register ESC Write Enable (0x0030)

ESC20	ET1100	ET1200	IP Core
~~read~~			read: V2.4.0/ V2.04a

Bit	Description	ECAT	PDI	Reset Value
0	If ESC write protection is enabled, this register has to be written in the same Ethernet frame (value does not matter) before other writes to this station are allowed. This bit is self-clearing at the beginning of the next frame (SOF), or if ESC Write Protection is disabled.	r/w	r/-	0
7:1	Reserved, write 0	r/-	r/-	0

2.14 ESC Write Protection (0x0031)

Table 15: Register ESC Write Protection (0x0031)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	Write protect: 0: Protection disabled 1: Protection enabled All areas are write-protected, except for 0x0030.	r/w	r/-	0
7:1	Reserved, write 0	r/-	r/-	0

2.15 ESC Reset ECAT (0x0040)

Table 16: Register ESC Reset ECAT (0x0040)

~~ESC20~~	**ET1100**	**ET1200**	IP Core

Bit	Description	ECAT	PDI	Reset Value
Write				
7:0	A reset is asserted after writing the reset sequence 0x52 (‘R’), 0x45 (‘E’) and 0x53 (‘S’) in this register with 3 consecutive frames. Any other frame which does not continue the sequence by writing the next expected value will cancel the reset procedure. NOTE: Some ESCs require to repeat this sequence until the ESC is actually reset. Do not use VLAN tagged frames.	r/w	r/-	0
Read				
1:0	Progress of the reset procedure: 00: initial/reset state 01: after writing 0x52 (‘R’), when previous state was 00 10: after writing 0x45 (‘E’), when previous state was 01 11: after writing 0x53 (‘S’), when previous state was 10. This value must not be observed because the ESC enters reset when this state is reached, resulting in state 00.	r/w	r/-	00
7:2	Reserved, write 0	r/-	r/-	0

2.16 ESC Reset PDI (0x0041)

Table 17: Register ESC Reset PDI (0x0041)

ESC20	ET1100	ET1200	IP Core
			V2.2.0/ V2.02a

Bit	Description	ECAT	PDI	Reset Value
Write				
7:0	A reset is asserted after writing the reset sequence 0x52 (‘R’), 0x45 (‘E’) and 0x53 (‘S’) in this register with 3 consecutive commands. Any other command which does not continue the sequence by writing the next expected value will cancel the reset procedure.	r/-	r/w	0
Read				
1:0	Progress of the reset procedure: 00: initial/reset state 01: after writing 0x52 (‘R’), when previous state was 00 10: after writing 0x45 (‘E’), when previous state was 01 11: after writing 0x53 (‘S’), when previous state was 10. This value must not be observed because the ESC enters reset when this state is reached, resulting in state 00.	r/-	r/w	00
7:2	Reserved, write 0	r/-	r/-	0

2.17 ESC DL Control (0x0100:0x0103)

Table 18: Register ESC DL Control (0x0100:0x0103)

ESC20	ET1100	ET1200	IP Core
~~[1]~~ ~~[23:19]~~	[23:20] -0003	[23:20] -0003	[24] config. before V2.4.0/ V2.04a [23:20] V2.4.3/ V2.04d ~~[19]~~

Bit	Description	ECAT	PDI	Reset Value
0	Forwarding rule: 0: Forward non-EtherCAT frames: EtherCAT frames are processed, non-EtherCAT frames are forwarded without processing or modification. The source MAC address is not changed for any frame. 1: Destroy non-EtherCAT frames: EtherCAT frames are processed, non-EtherCAT frames are destroyed. The source MAC address is changed by the Processing Unit for every frame (SOURCE_MAC[1] is set to 1 – locally administered address).	r/w	r/-	1
1	Temporary use of settings in 0x0100:0x0103[8:15]: 0: permanent use 1: use for about 1 second, then revert to previous settings	r/w	r/-	0
7:2	Reserved, write 0	r/-	r/-	0
9:8	Loop Port 0: 00: Auto 01: Auto Close 10: Open 11: Closed NOTE: Loop open means sending/receiving over this port is enabled, loop closed means sending/receiving is disabled and frames are forwarded to the next open port internally. Auto: loop closed at link down, opened at link up Auto Close: loop closed at link down, opened with writing 01 again after link up (or receiving a valid Ethernet frame at the closed port) Open: loop open regardless of link state Closed: loop closed regardless of link state	r/w*	r/-	00
11:10	Loop Port 1: 00: Auto 01: Auto Close 10: Open 11: Closed	r/w*	r/-	00

Bit	Description	ECAT	PDI	Reset Value
13:12	Loop Port 2: 00: Auto 01: Auto Close 10: Open 11: Closed	r/w*	r/-	00
15:14	Loop Port 3: 00: Auto 01: Auto Close 10: Open 11: Closed	r/w*	r/-	ET1200: 11 others: 00
18:16	RX FIFO Size (ESC delays start of forwarding until FIFO is at least half full). RX FIFO Size/RX delay reduction** : Value: EBUS: MII: 0: -50 ns -40 ns (-80 ns***) 1: -40 ns -40 ns (-80 ns***) 2: -30 ns -40 ns 3: -20 ns -40 ns 4: -10 ns no change 5: no change no change 6: no change no change 7: default default NOTE: EEPROM value is only taken over at first EEPROM load after power-on or reset	r/w	r/-	IP Core since V2.4.3/V2.04d: 7, later EEPROM word 5[11:9] inverted Others: 7
19	EBUS Low Jitter: 0: Normal jitter 1: Reduced jitter	r/w	r/-	0
21:20	Reserved, write 0	r/w	r/-	0, later EEPROM word 5[5:4]
22	EBUS remote link down signaling time: 0: Default (~660 ms) 1: Reduced (~80 µs)	r/w	r/-	0, later EEPROM word 5[6]
23	Reserved, write 0	r/w	r/-	0, later EEPROM word 5[7]
24	Station alias: 0: Ignore Station Alias 1: Alias can be used for all configured address command types (FPRD, FPWR, …)	r/w	r/-	0
31:25	Reserved, write 0	r/-	r/-	0

* Loop configuration changes are delayed until the end of a currently received or transmitted frame at the port.

** The possibility of RX FIFO Size reduction depends on the clock source accuracy of the ESC and of every connected EtherCAT/Ethernet devices (master, slave, etc.). RX FIFO Size of 7 is sufficient for 100ppm accuracy, FIFO Size 0 is possible with 25ppm accuracy (frame size of 1518/1522 Byte).

*** Reduction by 80 ns for IP Core since V3.0.0/V3.00c only, otherwise reduction by 40 ns.

2.18 Physical Read/Write Offset (0x0108:0x0109)

Table 19: Register Physical Read/Write Offset (0x0108:0x0109)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	This register is used for ReadWrite commands in Device Addressing mode (FPRW, APRW, BRW). The internal read address is directly taken from the offset address field of the EtherCAT datagram header, while the internal write address is calculated by adding the Physical Read/Write Offset value to the offset address field. Internal read address = ADR, internal write address = ADR + R/W-Offset	r/w	r/-	0

2.19 ESC DL Status (0x0110:0x0111)

Table 20: Register ESC DL Status (0x0110:0x0111)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	PDI operational/EEPROM loaded correctly: 0: EEPROM not loaded, PDI not operational (no access to Process Data RAM) 1: EEPROM loaded correctly, PDI operational (access to Process Data RAM)	r*/-	r/-	0
1	PDI Watchdog Status: 0: Watchdog expired 1: Watchdog reloaded	r*/-	r/-	0
2	Enhanced Link detection: 0: Deactivated for all ports 1: Activated for at least one port NOTE: EEPROM value is only transferred into this register at first EEPROM load after power-on or reset	r*/-	r/-	ET1100/ET1200: 1 until first EEPROM load, then EEPROM word 0[9] IP Core with feature: 1 until first EEPROM load, then 0 if EEPROM word 0[9]=0 and EEPROM word 0[15:12]=0x0, else 1 Others: 0
3	Reserved	r*/-	r/-	0
4	Physical link on Port 0: 0: No link 1: Link detected	r*/-	r/-	0
5	Physical link on Port 1: 0: No link 1: Link detected	r*/-	r/-	0
6	Physical link on Port 2: 0: No link 1: Link detected	r*/-	r/-	0
7	Physical link on Port 3: 0: No link 1: Link detected	r*/-	r/-	0
8	Loop Port 0: 0: Open 1: Closed	r*/-	r/-	0
9	Communication on Port 0: 0: No stable communication 1: Communication established	r*/-	r/-	0
10	Loop Port 1: 0: Open 1: Closed	r*/-	r/-	0
11	Communication on Port 1: 0: No stable communication 1: Communication established	r*/-	r/-	0

Bit	Description	ECAT	PDI	Reset Value
12	Loop Port 2: 0: Open 1: Closed	r*/-	r/-	0
13	Communication on Port 2: 0: No stable communication 1: Communication established	r*/-	r/-	0
14	Loop Port 3: 0: Open 1: Closed	r*/-	r/-	0
15	Communication on Port 3: 0: No stable communication 1: Communication established	r*/-	r/-	0

* Reading DL Status register from ECAT clears ECAT Event Request 0x0210[2]. Avoid reading DL Status register from PDI.

Table 21: Decoding port state in ESC DL Status register 0x0111 (typical modes only)

Register 0x0111	Port 3	Port 2	Port 1	Port 0
0x55	No link, closed	No link, closed	No link, closed	No link, closed
0x56	No link, closed	No link, closed	No link, closed	Link, open
0x59	No link, closed	No link, closed	Link, open	No link, closed
0x5A	No link, closed	No link, closed	Link, open	Link, open
0x65	No link, closed	Link, open	No link, closed	No link, closed
0x66	No link, closed	Link, open	No link, closed	Link, open
0x69	No link, closed	Link, open	Link, open	No link, closed
0x6A	No link, closed	Link, open	Link, open	Link, open
0x95	Link, open	No link, closed	No link, closed	No link, closed
0x96	Link, open	No link, closed	No link, closed	Link, open
0x99	Link, open	No link, closed	Link, open	No link, closed
0x9A	Link, open	No link, closed	Link, open	Link, open
0xA5	Link, open	Link, open	No link, closed	No link, closed
0xA6	Link, open	Link, open	No link, closed	Link, open
0xA9	Link, open	Link, open	Link, open	No link, closed
0xAA	Link, open	Link, open	Link, open	Link, open
0xD5	Link, closed	No link, closed	No link, closed	No link, closed
0xD6	Link, closed	No link, closed	No link, closed	Link, open
0xD9	Link, closed	No link, closed	Link, open	No link, closed
0xDA	Link, closed	No link, closed	Link, open	Link, open

2.20 AL Control (0x0120:0x0121)

Table 22: Register AL Control (0x0120:0x0121)

ESC20	ET1100	ET1200	IP Core
~~[15:5] (w ack)~~	~~(w ack)~~	~~(w ack)~~	[15:5] V2.4.0/ V2.04a

Bit	Description	ECAT	PDI	Reset Value
3:0	Initiate State Transition of the Device State Machine: 1: Request Init State 3: Request Bootstrap State 2: Request Pre-Operational State 4: Request Safe-Operational State 8: Request Operational State	r/(w)	r/ (w ack)*	1
4	Error Ind Ack: 0: No Ack of Error Ind in AL status register 1: Ack of Error Ind in AL status register	r/(w)	r/ (w ack)*	0
5	Device Identification: 0: No request 1: Device Identification request	r/(w)	r/ (w ack)*	0
15:6	Reserved, write 0	r/(w)	r/ (w ack)*	0

NOTE: AL Control register behaves like a mailbox if Device Emulation is off (0x0141[0]=0): The PDI has to read/write* the AL Control register after ECAT has written it. Otherwise ECAT cannot write again to the AL Control register. After Reset, AL Control register can be written by ECAT. (Regarding mailbox functionality, both low and high byte of the AL Control register trigger read/write functions, e.g., reading 0x0121 is sufficient to make this register writable again)
If Device Emulation is on, the AL Control register can always be written, its content is copied to the AL Status register.

* PDI register function acknowledge by Write command is disabled: Reading AL Control from PDI clears AL Event Request 0x0220[0]. Writing to this register from PDI is not possible.
PDI register function acknowledge by Write command is enabled: Writing AL Control from PDI clears AL Event Request 0x0220[0]. Writing to this register from PDI is possible; write value is ignored (write 0).

2.21 AL Status (0x0130:0x0131)

Table 23: Register AL Status (0x0130:0x0131)

ESC20	ET1100	ET1200	IP Core
~~[15:5]~~			[15:5] V2.4.0/ V2.04a

Bit	Description	ECAT	PDI	Reset Value
3:0	Actual State of the Device State Machine: 1: Init State 3: Bootstrap State 2: Pre-Operational State 4: Safe-Operational State 8: Operational State	r*/-	r/(w)	1
4	Error Ind: 0: Device is in State as requested or Flag cleared by command 1: Device has not entered requested State or changed State as result of a local action	r*/-	r/(w)	0
5	Device Identification: 0: Device Identification not valid 1: Device Identification loaded	r*/-	r/(w)	0
15:6	Reserved, write 0	r*/-	r/(w)	0

NOTE: AL Status register is only writable from PDI if Device Emulation is off (0x0141[0]=0), otherwise AL Status register will reflect AL Control register values. Avoid reading AL Status register from PDI.

* Reading AL Status from ECAT clears ECAT Event Request 0x0210[3].

2.22 AL Status Code (0x0134:0x0135)

Table 24: Register AL Status Code (0x0134:0x0135)

ESC20	ET1100	ET1200	IP Core
			V1.0.0/ V1.01b

Bit	Description	ECAT	PDI	Reset Value
15:0	AL Status Code	r/-	r/w	0

2.23 RUN LED Override (0x0138)

Table 25: Register RUN LED Override (0x0138)

ESC20	ET1100	ET1200	IP Core
			V2.3.0/ V2.03a

Bit	Description		ECAT	PDI	Reset Value
3:0	LED code: 0x0: Off 0x1: Flash 1x 0x2-0xC: Flash 2x – 12x 0xD: Blinking 0xE: Flickering 0xF: On	AL Status: Init (1) SafeOp (4) - PreOp (2) Bootstrap (3) Operational (8)	r/w	r/w	0
4	Enable Override: 0: Override disabled 1: Override enabled		r/w	r/w	0
7:5	Reserved, write 0		r/w	r/w	0

NOTE: Changes to AL Status register (0x0130) with valid values will disable RUN LED Override (0x0138[4]=0). The value read in this register always reflects current LED output.

2.24 ERR LED Override (0x0139)

Table 26: Register ERR LED Override (0x0139)

ESC20	ET1100	ET1200	IP Core
			V2.3.0/ V2.03a

Bit	Description	ECAT	PDI	Reset Value
3:0	LED code: 0x0: Off 0x1-0xC: Flash 1x – 12x 0xD: Blinking 0xE: Flickering 0xF: On	r/w	r/w	0
4	Enable Override: 0: Override disabled 1: Override enabled	r/w	r/w	0
7:5	Reserved, write 0	r/w	r/w	0

NOTE: New error conditions will disable ERR LED Override (0x0139[4]=0). The value read in this register always reflects current LED output.

2.25 PDI Control (0x0140)

Table 27: Register PDI Control (0x0140)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
7:0	Process data interface: 0x00: Interface deactivated (no PDI) 0x01: 4 Digital Input 0x02: 4 Digital Output 0x03: 2 Digital Input and 2 Digital Output 0x04: Digital I/O 0x05: SPI Slave 0x06: Oversampling I/O 0x07: EtherCAT Bridge (port 3) 0x08: 16 Bit asynchronous Microcontroller interface 0x09: 8 Bit asynchronous Microcontroller interface 0x0A: 16 Bit synchronous Microcontroller interface 0x0B: 8 Bit synchronous Microcontroller interface 0x10: 32 Digital Input and 0 Digital Output 0x11: 24 Digital Input and 8 Digital Output 0x12: 16 Digital Input and 16 Digital Output 0x13: 8 Digital Input and 24 Digital Output 0x14: 0 Digital Input and 32 Digital Output 0x80: On-chip bus Others: Reserved	r/-	r/-	IP Core: Depends on configuration Others: 0, later EEPROM word 0

2.26 ESC Configuration (0x0141)

Table 28: Register ESC Configuration (0x0141)

ESC20	ET1100	ET1200	IP Core
~~[7:1]~~	~~[7:4]~~	~~[7:2]~~	[7:4] V2.2.0/ V2.02a

Bit	Description	ECAT	PDI	Reset Value
0	Device emulation (control of AL status): 0: AL status register has to be set by PDI 1: AL status register will be set to value written to AL control register	r/-	r/-	IP Core: 1 with Digital I/O PDI, PDI_EMULATION pin with µC/On-chip bus Others: 0, later EEPROM word 0
1	Enhanced Link detection all ports: 0: disabled (if bits [7:4]=0) 1: enabled at all ports (overrides bits [7:4])	r/-	r/-	1, later EEPROM word 0
2	Distributed Clocks SYNC Out Unit: 0: disabled (power saving) 1: enabled	r/-	r/-	IP Core: Depends on configuration Others: 0, later EEPROM word 0
3	Distributed Clocks Latch In Unit: 0: disabled (power saving) 1: enabled	r/-	r/-	
4	Enhanced Link port 0: 0: disabled (if bit 1=0) 1: enabled	r/-	r/-	1, later EEPROM word 0
5	Enhanced Link port 1: 0: disabled (if bit 1=0) 1: enabled	r/-	r/-	
6	Enhanced Link port 2: 0: disabled (if bit 1=0) 1: enabled	r/-	r/-	
7	Enhanced Link port 3: 0: disabled (if bit 1=0) 1: enabled	r/-	r/-	

NOTE: EEPROM values of bits 1, 4, 5, 6, and 7 are only transferred into this register at first EEPROM load after power-on or reset.

2.27 PDI Information (0x014E:0x014F)

Table 29: Register PDI Information (0x014E:0x014F)

~~ESC20~~	~~ET1100~~	~~ET1200~~	IP Core
			V3.0.0/ V3.00a

Bit	Description	ECAT	PDI	Reset Value
0	PDI function acknowledge by write: 0: Disabled 1: Enabled	r/-	r/-	IP Core: Depends on configuration
1	ESC configuration area loaded from EEPROM: 0: not loaded 1: loaded	r/-	r/-	0
2	PDI active: 0: PDI not active 1: PDI active	r/-	r/-	
3	PDI configuration invalid: 0: PDI configuration ok 1: PDI configuration invalid	r/-	r/-	
15:4	Reserved	r/-	r/-	

2.28 PDI Configuration (0x0150:0x0153)

The PDI configuration register 0x0150 and the extended PDI configuration registers 0x0152:0x0153 depend on the selected PDI. The Sync/Latch[1:0] PDI configuration register 0x0151 is independent of the selected PDI.

Table 30: PDI Configuration Register overview

PDI number	PDI name	Configuration registers	
0x04	Digital I/O	0x0150	0x0152:0x0153
0x05	SPI Slave	0x0150	0x0152:0x0153
0x07	EtherCAT Bridge (port 3)	0x0150	0x0152:0x0153
0x08/0x09	8/16Bit asynchronous Microcontroller	0x0150	0x0152:0x0153
0x0A/0x0B	8/16Bit synchronous Microcontroller	0x0150	0x0152:0x0153
0x80	On-chip bus	0x0150	0x0152:0x0153
Sync/Latch[1:0] PDI Configuration			
-	Sync/Latch PDI Configuration	0x0151	

2.28.1 PDI Digital I/O configuration

Table 31: Register PDI Digital I/O configuration (0x0150)

~~ESC20~~	**ET1100**	**ET1200**	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	OUTVALID polarity: 0: Active high 1: Active low	r/-	r/-	IP Core: 0 Others: 0, later EEPROM word 1
1	OUTVALID mode: 0: Output event signaling 1: Process Data Watchdog trigger (WD_TRIG) signaling on OUTVALID pin (see SyncManager). Output data is updated if watchdog is triggered. Overrides 0x0150[7:6]	r/-	r/-	
2	Unidirectional/Bidirectional mode*: 0: Unidirectional mode: input/output direction of pins configured individually 1: Bidirectional mode: all I/O pins are bidirectional, direction configuration is ignored	r/-	r/-	IP Core: 1 Others: 0, later EEPROM word 1
3	Watchdog behavior: 0: Outputs are reset immediately after watchdog expires 1: Outputs are reset with next output event that follows watchdog expiration	r/-	r/-	IP Core: 0 Others: 0, later EEPROM word 1
5:4	Input DATA is sampled at 00: Start of Frame[2] 01: Rising edge of LATCH_IN 10: DC SYNC0 event[2] 11: DC SYNC1 event[2]	r/-	r/-	IP Core: Depends on configuration Others: 0, later EEPROM word 1
7:6	Output DATA is updated at 00: End of Frame 01: reserved 10: DC SYNC0 event 11: DC SYNC1 event If 0x0150[1]=1, output DATA is updated at Process Data Watchdog trigger event (0x0150[7:6] are ignored)	r/-	r/-	IP Core: Depends on configuration Others: 0, later EEPROM word 1

* IP Core: I/O direction depends on configuration, bidirectional mode is not supported.

Table Register Sync/Latch[1:0] PDI Configuration (0x0151) moved to chapter 2.28.7

[2] ET1200: LATCH_IN/SOF reflects Start of Frame (SOF) if input data is sampled with SOF or DC SYNC events.

Table 32: Register PDI Digital I/O extended configuration (0x0152:0x0153)

~~ESC20~~	**ET1100**	**ET1200**	IP Core
		~~[15:8]~~	

Bit	Description	ECAT	PDI	Reset Value
	Digital I/Os are configured in pairs as inputs or outputs: 0: Input 1: Output NOTE: Reserved in bidirectional mode, set to 0. Configuration bits for unavailable I/Os are reserved, set EEPROM value to 0.			
0	Direction of I/O[1:0]	r/-	r/-	IP Core: Depends on configuration Others: 0, later EEPROM word 3
1	Direction of I/O[3:2]			
2	Direction of I/O[5:4]			
3	Direction of I/O[7:6]			
4	Direction of I/O[9:8]			
5	Direction of I/O[11:10]			
6	Direction of I/O[13:12]			
7	Direction of I/O[15:14]			
8	Direction of I/O[17:16]			
9	Direction of I/O[19:18]			
10	Direction of I/O[21:20]			
11	Direction of I/O[23:22]			
12	Direction of I/O[25:24]			
13	Direction of I/O[27:26]			
14	Direction of I/O[29:28]			
15	Direction of I/O[31:30]			

2.28.2 PDI SPI Slave Configuration

Table 33: Register PDI SPI Slave Configuration (0x0150)

	ESC20	ET1100	ET1200	IP Core
	~~[3:2], [7:6]~~	~~[7:6]~~	~~[7:6]~~	~~[7:6]~~

Bit	Description	ECAT	PDI	Reset Value
1:0	SPI mode: 00: SPI mode 0 01: SPI mode 1 10: SPI mode 2 11: SPI mode 3 NOTE: SPI mode 3 is recommended for Slave Sample Code NOTE: SPI status flag is not available in SPI modes 0 and 2 with normal data out sample.	r/-	r/-	IP Core: Depends on configuration Others: 0, later EEPROM word 1
3:2	SPI_IRQ output driver/polarity: 00: Push-Pull active low 01: Open Drain (active low) 10: Push-Pull active high 11: Open Source (active high)	r/-	r/-	
4	SPI_SEL polarity: 0: Active low 1: Active high	r/-	r/-	
5	Data Out sample mode: 0: Normal sample (SPI_DO and SPI_DI are sampled at the same SPI_CLK edge) 1: Late sample (SPI_DO and SPI_DI are sampled at different SPI_CLK edges)	r/-	r/-	
7:6	Reserved, set EEPROM value to 0	r/-	r/-	

Table Register Sync/Latch[1:0] PDI Configuration (0x0151) moved to chapter 2.28.7

Table 34: Register PDI SPI Slave extended configuration (0x0152:0x0153)

	~~ESC20~~	ET1100	ET1200	IP Core
		~~[15:0]~~	~~[15:0]~~	~~[15:0]~~

Bit	Description	ECAT	PDI	Reset Value
15:0	Reserved, set EEPROM value to 0	r/-	r/-	IP Core: 0 Others: 0, later EEPROM word 3

2.28.3 PDI 8/16Bit asynchronous Microcontroller configuration

Table 35: Register PDI asynchronous Microcontroller Configuration (0x0150)

	ESC20	ET1100	~~ET1200~~	IP Core
	~~[7:4]~~			

Bit	Description	ECAT	PDI	Reset Value
1:0	BUSY output driver/polarity: 00: Push-Pull active low 01: Open Drain (active low) 10: Push-Pull active high 11: Open Source (active high) NOTE: Push-Pull: no CS → not BUSY (driven) Open Drain/Source: no CS → BUSY open	r/-	r/-	IP Core: Depends on configuration Others: 0, later EEPROM word 1
3:2	IRQ output driver/polarity: 00: Push-Pull active low 01: Open Drain (active low) 10: Push-Pull active high 11: Open Source (active high)	r/-	r/-	
4	BHE/Byte Enable polarity: 0: Active low 1: Active high	r/-	r/-	IP Core: 0 Others: 0, later EEPROM word 1
6:5	Reserved, set EEPROM value to 0	r/-	r/-	
7	RD Polarity: 0: Active low 1: Active high	r/-	r/-	

Table Register Sync/Latch[1:0] PDI Configuration (0x0151) moved to chapter 2.28.7

Table 36: Register PDI Asynchronous Microcontroller extended Configuration (0x0152:0x0153)

~~ESC20~~	ET1100	~~ET1200~~	IP Core
	~~[15:1]~~		[0] V2.2.0/ V2.02a [1] V2.3.0/ V2.03a

Bit	Description	ECAT	PDI	Reset Value
0	Read BUSY delay: 0: Normal read BUSY output 1: Delayed read BUSY output	r/-	r/-	IP Core: 0 Others: 0, later EEPROM word 3
1	Perform internal write at: 0: End of write access 1: Beginning of write access	r/-	r/-	
15:2	Reserved, set EEPROM value to 0	r/-	r/-	

2.28.4 PDI 8/16Bit synchronous Microcontroller configuration

Table 37: Register PDI Synchronous Microcontroller Configuration (0x0150)

~~ESC20~~ **ET1100** ~~ET1200~~ ~~IP Core~~

Bit	Description	ECAT	PDI	Reset Value
1:0	TA output driver/polarity: 00: Push-Pull active low 01: Open Drain (active low) 10: Push-Pull active high 11: Open Source (active high) NOTE: Push-Pull: no CS → no TA (driven) Open Drain/Source: no CS → TA open	r/-	r/-	0, later EEPROM word 1
3:2	IRQ output driver/polarity: 00: Push-Pull active low 01: Open Drain (active low) 10: Push-Pull active high 11: Open Source (active high)	r/-	r/-	
4	BHE/Byte Enable polarity: 0: Active low 1: Active high	r/-	r/-	
5	ADR(0) polarity: 0: Active high 1: Active low	r/-	r/-	
6	Byte access mode: 0: BHE or Byte Enable mode 1: Transfer Size mode	r/-	r/-	
7	TS Polarity: 0: Active low 1: Active high	r/-	r/-	

Table Register Sync/Latch[1:0] PDI Configuration (0x0151) moved to chapter 2.28.7

Table 38: Register PDI Synchronous Microcontroller extended Configuration (0x0152:0x0153)

ESC20	**ET1100**	ET1200	IP Core
	[7:0]		

Bit	Description	ECAT	PDI	Reset Value
7:0	Reserved, set EEPROM value to 0	r/-	r/-	0, later EEPROM word 3
8	Write data valid: 0: Write data valid one clock cycle after CS 1: Write data valid together with CS	r/-	r/-	
9	Read mode: 0: Use Byte Selects for read accesses 1: Ignore Byte Selects for read accesses, always read full PDI width	r/-	r/-	
10	CS mode: 0: Sample CS with rising edge of CPU_CLK 1: Sample CS with falling edge of CPU_CLK	r/-	r/-	
11	TA/IRQ mode: 0: Update TA/IRQ with rising edge of CPU_CLK 1: Update TA/IRQ with falling edge of CPU_CLK	r/-	r/-	
15:12	Reserved, set EEPROM value to 0	r/-	r/-	

2.28.5 EtherCAT Bridge (port 3)

Table 39: Register EtherCAT Bridge configuration (0x0150)

ESC20	ET1100	**ET1200**	IP Core
		[1]	

Bit	Description	ECAT	PDI	Reset Value
0	Bridge port physical layer: 0: EBUS 1: MII	r/-	r/-	0, later EEPROM word 1
1	Initial port state: 0: Always closed (0x0100[15:14]=11) 1: Auto (0x0100[15:14]=00)	r/-	r/-	
7:2	Reserved, set EEPROM value to 0	r/-	r/-	

Table Register Sync/Latch[1:0] PDI Configuration (0x0151) moved to chapter 2.28.7

Table 40: Register EtherCAT Bridge extended configuration (0x0152:0x0153)

ESC20	ET1100	**ET1200**	IP Core
		[15:8]	

Bit	Description	ECAT	PDI	Reset Value
15:0	Reserved, set EEPROM value to 0	r/-	r/-	0, later EEPROM word 3

2.28.6 PDI On-chip bus configuration

Table 41: Register PDI On-chip bus configuration (0x0150)

~~ESC20~~	~~ET1100~~	~~ET1200~~	IP Core

Bit	Description	ECAT	PDI	Reset Value
4:0	On-chip bus clock: 0: asynchronous 1-31: synchronous multiplication factor (N * 25 MHz)	r/-	r/-	IP Core: Depends on configuration
7:5	On-chip bus: 000: Intel® Avalon® 001: AXI® 010: Xilinx® PLB v4.6 100: Xilinx OPB others: reserved	r/-	r/-	

Table Register Sync/Latch[1:0] PDI Configuration (0x0151) moved to chapter 2.28.7

Table 42: Register PDI On-chip bus extended configuration (0x0152:0x0153)

~~ESC20~~	~~ET1100~~	~~ET1200~~	IP Core
			V1.1.1/ V2.00a

Bit	Description	ECAT	PDI	Reset Value
1:0	Read prefetch size (in cycles of PDI width): 0: 4 cycles 1: 1 cycle (typical) 2: 2 cycles 3: Reserved	r/-	r/-	IP Core: Depends on configuration
7:2	Reserved	r/-	r/-	
10:8	On-chip bus sub-type for AXI: 000: AXI3 001: AXI4 010: AXI4 LITE others: reserved	r/-	r/-	
15:11	Reserved	r/-	r/-	

2.28.7 Sync/Latch Configuration

Table 43: Register Sync/Latch Configuration (0x0151)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
1:0	SYNC0 output driver/polarity: 00: Push-Pull active low 01: Open Drain (active low) 10: Push-Pull active high 11: Open Source (active high)	r/-	r/-	IP Core: 10 Others: 00, later EEPROM word 1	
2	SYNC0/LATCH0 configuration*: 0: LATCH0 Input 1: SYNC0 Output	r/-	r/-	IP Core: 1 Others: 0, later EEPROM word 1	
3	SYNC0 mapped to AL Event Request register 0x0220[2]: 0: Disabled 1: Enabled	r/-	r/-	IP Core: Depends on configuration Others: 0, later EEPROM word 1	
5:4	SYNC1 output driver/polarity: 00: Push-Pull active low 01: Open Drain (active low) 10: Push-Pull active high 11: Open Source (active high)	r/-	r/-	IP Core: 10 Others: 00, later EEPROM word 1	
6	SYNC1/LATCH1 configuration*: 0: LATCH1 input 1: SYNC1 output	r/-	r/-	IP Core: 1 Others: 0, later EEPROM word 1	
7	SYNC1 mapped to AL Event Request register 0x0220[3]: 0: Disabled 1: Enabled	r/-	r/-	IP Core: Depends on configuration Others: 0, later EEPROM word 1	

* The IP Core has concurrent SYNC[1:0] outputs and LATCH[1:0] inputs, independent of this configuration.

2.29 ECAT Event Mask (0x0200:0x0201)

Table 44: Register ECAT Event Mask (0x0200:0x0201)

ESC20	ET1100	ET1200	IP Core
			write config. V2.4.0/ V2.04a writable

Bit	Description	ECAT	PDI	Reset Value
15:0	ECAT Event masking of the ECAT Event Request Events for mapping into ECAT event field of EtherCAT frames: 0: Corresponding ECAT Event Request register bit is not mapped 1: Corresponding ECAT Event Request register bit is mapped	r/w	r/-	0

2.30 PDI AL Event Mask (0x0204:0x0207)

Table 45: Register PDI AL Event Mask (0x0204:0x0207)

ESC20	ET1100	ET1200	IP Core
			write config.

Bit	Description	ECAT	PDI	Reset Value
31:0	AL Event masking of the AL Event Request register Events for mapping to PDI IRQ signal: 0: Corresponding AL Event Request register bit is not mapped 1: Corresponding AL Event Request register bit is mapped	r/-	r/w	0x00FF:0xFF0F

2.31 ECAT Event Request (0x0210:0x0211)

Table 46: Register ECAT Event Request (0x0210:0x0211)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	DC Latch event: 0: No change on DC Latch Inputs 1: At least one change on DC Latch Inputs (Bit is cleared by reading DC Latch event times from ECAT for ECAT-controlled Latch Units, so that Latch 0/1 Status 0x09AE:0x09AF indicates no event)	r/-	r/-	0
1	Reserved	r/-	r/-	0
2	DL Status event: 0: No change in DL Status 1: DL Status change (Bit is cleared by reading out DL Status 0x0110:0x0111 from ECAT)	r/-	r/-	0
3	AL Status event: 0: No change in AL Status 1: AL Status change (Bit is cleared by reading out AL Status 0x0130:0x0131 from ECAT)	r/-	r/-	0
4 5 … 11	Mirrors values of each SyncManager Status: 0: No Sync Channel 0 event 1: Sync Channel 0 event pending 0: No Sync Channel 1 event 1: Sync Channel 1 event pending … 0: No Sync Channel 7 event 1: Sync Channel 7 event pending	r/-	r/-	0
15:12	Reserved	r/-	r/-	0

2.32 AL Event Request (0x0220:0x0223)

Table 47: Register AL Event Request (0x0220:0x0223)

ESC20	ET1100	ET1200	IP Core
~~[6:4]~~	~~[6:5]~~	~~[6:5]~~	[5:4] V2.0.0/ V2.00a; [6] V2.3.0/ V2.03a

Bit	Description	ECAT	PDI	Reset Value
0	AL Control event: 0: No AL Control Register change 1: AL Control Register has been written[3] (Bit is cleared by reading AL Control register 0x0120:0x0121 from PDI)	r/-	r/-	0
1	DC Latch event: 0: No change on DC Latch Inputs 1: At least one change on DC Latch Inputs (Bit is cleared by reading DC Latch event times from PDI, so that Latch 0/1 Status 0x09AE:0x09AF indicates no event. Available if Latch Unit is PDI-controlled)	r/-	r/-	0
2	State of DC SYNC0 (if register 0x0151[3]=1): (Bit is cleared by reading SYNC0 status 0x098E from PDI, use only in Acknowledge mode)	r/-	r/-	0
3	State of DC SYNC1 (if register 0x0151[7]=1): (Bit is cleared by reading of SYNC1 status 0x098F from PDI, use only in Acknowledge mode)	r/-	r/-	0
4	SyncManager activation register (SyncManager register offset 0x6) changed: 0: No change in any SyncManager 1: At least one SyncManager changed (Bit is cleared by reading SyncManager Activation registers 0x0806 etc. from PDI)	r/-	r/-	0
5	EEPROM Emulation: 0: No command pending 1: EEPROM command pending (Bit is cleared by acknowledging the command in EEPROM Control/Status register 0x0502:0x0503[10:8] from PDI)	r/-	r/-	0
6	Watchdog Process Data: 0: Has not expired 1: Has expired (Bit is cleared by reading Watchdog Status Process Data 0x0440 from PDI)	r/-	r/-	0
7	Reserved	r/-	r/-	0

[3] AL control event is only generated if PDI emulation is turned off (ESC Configuration 0 register 0x0141[0]=0)

Bit	Description	ECAT	PDI	Reset Value
8 9 …. 23	SyncManager interrupts (SyncManager register offset 0x5, bit [0] or [1]): 0: No SyncManager 0 interrupt 1: SyncManager 0 interrupt pending 0: No SyncManager 1 interrupt 1: SyncManager 1 interrupt pending … 0: No SyncManager 15 interrupt 1: SyncManager 15 interrupt pending	r/-	r/-	0
31:24	Reserved	r/-	r/-	0

2.33 RX Error Counter (0x0300:0x0307)

Table 48: Register RX Error Counter Port y (0x0300+y*2:0x0301+y*2)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
7:0	Invalid frame counter of Port y (counting is stopped when 0xFF is reached).	r/ w(clr)	r/-	0
15:8	RX Error counter of Port y (counting is stopped when 0xFF is reached).	r/ w(clr)	r/-	0

NOTE: Error Counters 0x0300-0x030B are cleared if one of the implemented RX Error counters 0x0300-0x030B is written (preferably 0x0300). Write value is ignored (write 0). Errors are only counted if the loop of the port is open.

2.34 Forwarded RX Error Counter (0x0308:0x030B)

Table 49: Register Forwarded RX Error Counter Port y (0x0308+y)

~~ESC20~~	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
7:0	Forwarded error counter of Port y (counting is stopped when 0xFF is reached).	r/ w(clr)	r/-	0

NOTE: Error Counters 0x0300-0x30B are cleared if one of the implemented RX Error counters 0x0300-0x030B is written (preferably 0x0300). Write value is ignored (write 0). Errors are only counted if the loop of the port is open.

2.35 ECAT Processing Unit Error Counter (0x030C)

Table 50: Register ECAT Processing Unit Error Counter (0x030C)

~~ESC20~~	ET1100	~~ET1200~~	IP Core

Bit	Description	ECAT	PDI	Reset Value
7:0	ECAT Processing Unit error counter (counting is stopped when 0xFF is reached). Counts errors of frames passing the Processing Unit.	r/ w(clr)	r/-	0

NOTE: Error Counter 0x030C is cleared if error counter 0x030C is written. Write value is ignored (write 0).

2.36 PDI Error Counter (0x030D)

Table 51: Register PDI Error Counter (0x030D)

~~ESC20~~ **ET1100** ~~ET1200~~ IP Core

Bit	Description	ECAT	PDI	Reset Value
7:0	PDI Error counter (counting is stopped when 0xFF is reached). Counts if a PDI access has an interface error.	r/ w(clr)	r/-	0

NOTE: Error Counter 0x030D and Error Code 0x030E:0x030F are cleared if error counter 0x030D is written. Write value is ignored (write 0).

2.37 PDI Error Code (0x030E:0x030F)

2.37.1 SPI PDI Error Code

Table 52: Register SPI PDI Error Code (0x030E:0x030F)

~~ESC20~~	~~ET1100~~	~~ET1200~~	IP Core
			V2.3.0/ V2.03a ~~[15:8]~~

Bit	Description	ECAT	PDI	Reset Value
	Reasons for last PDI Error	r/-	r/-	0
2:0	Number of SPI clock cycles of whole access (modulo 8) causing PDI Error			
3	Busy violation during read access: 0: no error 1: error detected			
4	Read termination missing: 0: no error 1: error detected			
5	Access continued after read termination byte 0: no error 1: error detected			
7:6	0x030E[8]=0 or not supported: SPI command CMD[2:1] of access causing PDI error. 0x030E[8]=1: [SEL_MOSI:SEL_MISO] of access causing PDI error.			
15:8	reserved			

NOTE: Error Counter 0x030D and Error Code 0x030E:0x030F are cleared if error counter 0x030D is written. Write value is ignored (write 0).

2.37.2 Asynchronous/Synchronous Microcontroller PDI Error Code

Table 53: Register Microcontroller PDI Error Code (0x030E:0x030F)

~~ESC20~~	~~ET1100~~	~~ET1200~~	IP Core
			V2.3.0/ V2.03a ~~[15:8]~~

Bit	Description	ECAT	PDI	Reset Value
	Reasons for last PDI Error	r/-	r/-	0
0	Busy violation during read access 0: no error 1: error detected			
1	Busy violation during write access 0: no error 1: error detected			
2	Addressing error for a read access (odd address without BHE) 0: no error 1: error detected NOTE: for 16 bit µController PDI only			
3	Addressing error for a write access (odd address without BHE) 0: no error 1: error detected NOTE: for 16 bit µController PDI only			
15:4	Reserved			

NOTE: Error Counter 0x030D and Error Code 0x030E:0x030F are cleared if error counter 0x030D is written. Write value is ignored (write 0).

2.37.3 Avalon PDI Error Code

Table 54: Register Avalon PDI Error Code (0x030E:0x030F)

~~ESC20~~	~~ET1100~~	~~ET1200~~	IP Core
			V3.0.0/ V3.00c ~~[15:8]~~

Bit	Description	ECAT	PDI	Reset Value
	Reasons for last PDI Error	r/-	r/-	0
0	Both read and write signals active at the same time 0: no error 1: error detected			
15:1	Reserved			

NOTE: Error Counter 0x030D and Error Code 0x030E:0x030F are cleared if error counter 0x030D is written. Write value is ignored (write 0).

2.37.4 AXI PDI Error Code

Table 55: Register AXI PDI Error Code (0x030E:0x030F)

~~ESC20~~	~~ET1100~~	~~ET1200~~	IP Core
			V3.0.10/ V3.00k Patch 3 ~~[15:8]~~

Bit	Description	ECAT	PDI	Reset Value
	Reasons for last PDI Error	r/-	r/-	0
0	AWVALID removed without AW_READY: 0: no error 1: error detected			
1	WVALID removed without W_READY: 0: no error 1: error detected			
2	ARVALID removed without AR_READY: 0: no error 1: error detected			
3	AWSIZE too large: 0: no error 1: error detected			
4	ARSIZE too large: 0: no error 1: error detected			
15:5	Reserved			

NOTE: Error Counter 0x030D and Error Code 0x030E:0x030F are cleared if error counter 0x030D is written. Write value is ignored (write 0).

2.38 Lost Link Counter (0x0310:0x0313)

Table 56: Register Lost Link Counter Port y (0x0310+y)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
7:0	Lost Link counter of Port y (counting is stopped when 0xff is reached). Counts only if port is open and loop is Auto.	r/ w(clr)	r/-	0

NOTE: Lost Link Counters 0x0310-0x0313 are cleared if one of the implemented Lost Link Counters 0x0310-0x0313 is written (preferably 0x0310). Write value is ignored (write 0).

2.39 Watchdog Divider (0x0400:0x0401)

Table 57: Register Watchdog Divider (0x0400:0x0401)

	ESC20	ET1100	ET1200	IP Core
				write config.

Bit	Description	ECAT	PDI	Reset Value
15:0	Watchdog divider: Number of 25 MHz tics (minus 2) that represent the basic watchdog increment. (Default value is 100µs = 2498)	r/w	r/-	0x09C2

2.40 Watchdog Time PDI (0x0410:0x0411)

Table 58: Register Watchdog Time PDI (0x0410:0x0411)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	Watchdog Time PDI: number of basic watchdog increments (Default value with Watchdog divider 100µs means 100ms Watchdog)	r/w	r/-	0x03E8

Watchdog is disabled if Watchdog time is set to 0x0000. Watchdog starts counting again with every PDI access.

2.41 Watchdog Time Process Data (0x0420:0x0421)

Table 59: Register Watchdog Time Process Data (0x0420:0x0421)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	Watchdog Time Process Data: number of basic watchdog increments (Default value with Watchdog divider 100µs means 100ms Watchdog)	r/w	r/-	0x03E8

There is one Watchdog for all SyncManagers. Watchdog is disabled if Watchdog time is set to 0x0000. Watchdog starts counting again with every write access to SyncManagers with Watchdog Trigger Enable Bit set.

2.42 Watchdog Status Process Data (0x0440:0x0441)

Table 60: Register Watchdog Status Process Data (0x0440:0x0441)

	ESC20 (w ack)	ET1100 (w ack)	ET1200 (w ack)	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	Watchdog Status of Process Data (triggered by SyncManagers) 0: Watchdog Process Data expired 1: Watchdog Process Data is active or disabled	r/-	r/ (w ack)*	0
15:1	Reserved	r/-	r/ (w ack)*	0

* PDI register function acknowledge by Write command is disabled: Reading this register from PDI clears AL Event Request 0x0220[6]. Writing to this register from PDI is not possible.
PDI register function acknowledge by Write command is enabled: Writing this register from PDI clears AL Event Request 0x0220[6]. Writing to this register from PDI is possible; write value is ignored (write 0).

2.43 Watchdog Counter Process Data (0x0442)

Table 61: Register Watchdog Counter Process Data (0x0442)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
7:0	Watchdog Counter Process Data (counting is stopped when 0xFF is reached). Counts if Process Data Watchdog expires.	r/ w(clr)	r/-	0

NOTE: Watchdog Counters 0x0442-0x0443 are cleared if one of the Watchdog Counters 0x0442-0x0443 is written. Write value is ignored (write 0).

2.44 Watchdog Counter PDI (0x0443)

Table 62: Register Watchdog Counter PDI (0x0443)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
7:0	Watchdog PDI counter (counting is stopped when 0xFF is reached). Counts if PDI Watchdog expires.	r/ w(clr)	r/-	0

NOTE: Watchdog Counters 0x0442-0x0443 are cleared if one of the Watchdog Counters 0x0442-0x0443 is written. Write value is ignored (write 0).

2.45 SII EEPROM Interface (0x0500:0x050F)

Table 63: SII EEPROM Interface Register overview

Register Address	Length (Byte)	Description
0x0500	1	EEPROM Configuration
0x0501	1	EEPROM PDI Access State
0x0502:0x0503	2	EEPROM Control/Status
0x0504:0x0507	4	EEPROM Address
0x0508:0x050F	4/8	EEPROM Data

EtherCAT controls the SII EEPROM interface if EEPROM configuration register 0x0500[0]=0 and EEPROM PDI Access register 0x0501[0]=0, otherwise PDI controls the EEPROM interface.

In EEPROM emulation mode, the PDI executes pending EEPROM commands. The PDI has access to some registers while the EEPROM Interface is busy.

Table 64: Register EEPROM Configuration (0x0500)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	EEPROM control is offered to PDI: 0: no 1: yes (PDI has EEPROM control)	r/w	r/-	0
1	Force ECAT access: 0: Do not change Bit 0x0501[0] 1: Reset Bit 0x0501[0] to 0	r/w	r/-	0
7:2	Reserved, write 0	r/-	r/-	0

Table 65: Register EEPROM PDI Access State (0x0501)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	Access to EEPROM: 0: PDI releases EEPROM access 1: PDI takes EEPROM access (PDI has EEPROM control)	r/-	r/(w)	0
7:1	Reserved, write 0	r/-	r/-	0

NOTE: r/(w): write access is only possible if (0x0500[0]=1 or 0x0501[0]=1) and 0x0500[1]=0.

Table 66: Register EEPROM Control/Status (0x0502:0x0503)

		ESC20 [7]	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
0	ECAT write enable*2: 0: Write requests are disabled 1: Write requests are enabled This bit is always 1 if PDI has EEPROM control.	r/(w)	r/-	0	
4:1	Reserved, write 0	r/-	r/-	0	
5	EEPROM emulation: 0: Normal operation (I²C interface used) 1: PDI emulates EEPROM (I²C not used)	r/-	r/-	IP Core: depends on configuration Others: 0	
6	Supported number of EEPROM read bytes: 0: 4 Bytes 1: 8 Bytes	r/-	r/-	ET1100: 1 ET1200: 1 Others: 0	
7	Selected EEPROM Algorithm: 0: 1 address byte (1Kbit – 16Kbit EEPROMs) 1: 2 address bytes (32Kbit – 4 Mbit EEPROMs)	r/-	r/-	ESC20: 0*1 IP Core: depending on PROM_SIZE and features Others: PIN EEPROM size	
10:8	Command register*2: Write: Initiate command. Read: Currently executed command Commands: 000: No command/EEPROM idle (clear error bits) 001: Read 010: Write 100: Reload Others: Reserved/invalid commands (do not issue) EEPROM emulation only: after execution, PDI writes command value to indicate operation is ready.	r/(w)	r/(w) r/[w]	0	
11	Checksum Error in ESC Configuration Area: 0: Checksum ok 1: Checksum error EEPROM emulation for IP Core only: PDI writes 1 if a CRC failure has occurred for a reload command.	r/-	r/- r/[w]	0	
12	EEPROM loading status: 0: EEPROM loaded, device information ok 1: EEPROM not loaded, device information not available (EEPROM loading in progress or finished with a failure)	r/-	r/-	0	
13	Error Acknowledge/Command*3: 0: No error 1: Missing EEPROM acknowledge or invalid command EEPROM emulation only: PDI writes 1 if a temporary failure has occurred.	r/-	r/- r/[w]	0	
14	Error Write Enable*3: 0: No error 1: Write Command without Write enable	r/-	r/-	0	

Bit	Description	ECAT	PDI	Reset Value
15	Busy: 0: EEPROM Interface is idle 1: EEPROM Interface is busy	r/-	r/-	0

NOTE: r/(w): write access depends upon the assignment of the EEPROM interface (ECAT/PDI). Write access is blocked if EEPROM interface is busy (0x0502[15]=1).

NOTE: r/[w]: EEPROM emulation only: write access is possible if EEPROM interface is busy (0x0502[15]=1). PDI acknowledges pending commands by writing a 1 into the corresponding command register bits (0x0502[10:8]). General/temporary errors can be indicated by writing a 1 into the error bit 0x0502[13], CRC errors for Reload command can be indicated by writing a 1 into the error bit 0x0502[11]. Acknowledging clears AL Event Request 0x0220[5].

*[1] ESC20: configurable with pin EEPROM SIZE, but not readable in this register.

*[2] Write Enable bit 0 is self-clearing at the SOF of the next frame, Command bits [10:8] are self-clearing after the command is executed (EEPROM Busy ends). Writing “000” to the command register will also clear the error bits [14:13]. Command bits [10:8] are ignored if Error Acknowledge/Command is pending (bit 13).

*[3] Error bits are cleared by writing “000” (or any valid command) to Command Register Bits [10:8].

Table 67: Register EEPROM Address (0x0504:0x0507)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
31:0	EEPROM Address 0: First word (= 16 bit) 1: Second word … Actually used EEPROM Address bits: [9:0]: EEPROM size up to 16 Kbit [17:0]: EEPROM size 32 Kbit – 4 Mbit [31:0]: EEPROM Emulation	r/(w)	r/(w)	0

NOTE: r/(w): write access depends upon the assignment of the EEPROM interface (ECAT/PDI). Write access is blocked if EEPROM interface is busy (0x0502[15]=1).

Table 68: Register EEPROM Data (0x0508:0x050F [0x0508:0x050B])

	ESC20	ET1100	ET1200	IP Core
	~~[63:32]~~			~~[63:32]~~

Bit	Description	ECAT	PDI	Reset Value
15:0	EEPROM Write data (data to be written to EEPROM) or EEPROM Read data (data read from EEPROM, lower bytes)	r/(w)	r/(w) r/[w]	0
63:16	EEPROM Read data (data read from EEPROM, higher bytes)	r/-	r/- r/[w]	0

NOTE: r/(w): write access depends upon the assignment of the EEPROM interface (ECAT/PDI). Write access is blocked if EEPROM interface is busy (0x0502[15]=1).

NOTE: r/[w]: write access for EEPROM emulation if read or reload command is pending. See the following information for further details:

2.45.1 EEPROM emulation with 32 bit EEPROM data register (0x0502[6]=0)

Write access to the EEPROM Data register 0x0508:0x050B is possible if the EEPROM interface is busy (0x0502[15]=1). PDI places EEPROM read data in this register before the pending EEPROM Read command is acknowledged (writing to 0x0502[10:8]). For a Reload command, fill the EEPROM Data register with the values shown in the following table before acknowledging the command. These values are automatically transferred to the designated registers after the Reload command is acknowledged:

Table 69: Register EEPROM Data for 32 bit EEPROM Emulation Reload (0x0508:0x050B)

~~ESC20~~	~~ET1100~~	~~ET1200~~	IP Core
			[27:21] V2.4.3/ V2.04d

Bit	Description	ECAT	PDI	Reset Value
15:0	Configured Station Alias (NVRAM word 4[15:0], reloaded into 0x0012[15:0])	r/-	r/[w]	0
16	Enhanced Link Detection for all ports (NVRAM word 0[1], reloaded into 0x0141[1])	r/-	r/[w]	0
20:17	Enhanced Link Detection for individual ports (NVRAM word 0[7:4], reloaded into 0x0141[7:4])	r/-	r/[w]	0
24:21	ESC DL configuration (NVRAM word 5[7:4], loaded into register 0x0100[23:20])	r/-	r/[w]	0
27:25	FIFO Size reduction (NVRAM word 5[27:25], loaded into ESC DL Control register 0x0100[18:16]): 000: FIFO Size set to 7 001: FIFO Size set to 6 010: FIFO Size set to 5 011: FIFO Size set to 4 100: FIFO Size set to 3 101: FIFO Size set to 2 110: FIFO Size set to 1 111: FIFO Size set to 0 NOTE: This value sets the ESC DL control register only at the first EEPROM loading	r/-	r/[w]	0
31:28	Reserved, write 0	r/-	r/[w]	0

NOTE: r/[w]: write access for EEPROM emulation if read or reload command is pending.

2.46 MII Management Interface (0x0510:0x051B)

Table 70: MII Management Interface Register Overview

Register Address	Length (Byte)	Description
0x0510:0x0511	2	MII Management Control/Status
0x0512	1	PHY Address
0x0513	1	PHY Register Address
0x0514:0x0515	2	PHY Data
0x0516	1	MII Management ECAT Access State
0x0517	1	MII Management PDI Access State
0x0518:0x051B	4	PHY Port Status

ECAT controls the MII management interface if MII Management PDI Access register 0x0517[0]=0 or if 0x0517 is not available, otherwise PDI controls the MII management interface.
Exception for ET1100: PDI controls the MII management interface if Transparent Mode is enabled.

Table 71: Register MII Management Control/Status (0x0510:0x0511)

ESC20	ET1100	ET1200	IP Core
~~[10, 13]~~	~~[10, 13]~~	~~[10, 13]~~	[13] V2.0.0/ V2.00a [10] V3.3.0

Bit	Description	ECAT	PDI	Reset Value
0	Write enable*: 0: Write disabled 1: Write enabled This bit is always 1 if PDI has MI control. ET1100-0000/-0001 exception: Bit is not always 1 if PDI has MI control, and bit is writable by PDI.	r/(w)	r/-	0
1	Management Interface can be controlled by PDI (registers 0x0516-0x0517): 0: Only ECAT control 1: PDI control possible	r/-	r/-	IP Core since V2.0.0/V2.00a: 1 Others: 0
2	MI link detection and configuration: 0: Disabled for all ports 1: Enabled for at least one MII port, refer to PHY Port Status (0x0518 ff.) for details	r/-	r/-	IP Core: Depends on configuration Others: 0
7:3	PHY address of port 0 (this is equal to the PHY address offset, if the PHY addresses are consecutive) IP Core since V3.0.0/3.00c: Translation 0x0512[7]=0: Register 0x0510[7:3] shows PHY address of port 0 Translation 0x0512[7]=1: Register 0x0510[7:3] shows the PHY address which will be used for port 0-3 as requested by 0x0512[4:0] (valid values 0-3)	r/-	r/-	ET1100, ET1200: PHYAD_OFF IP Core: Depends on configuration Others: 0

Bit	Description	ECAT	PDI	Reset Value
9:8	Command register*: Write: Initiate command. Read: Currently executed command 00: No command/MI idle (clear error bits) 01: Read 10: Write Others: Reserved/invalid command (do not issue)	r/(w)	r/(w)	0
12:10	Reserved, write 0	r/-	r/-	0
13	Read error: 0: No read error 1: Read error occurred (PHY or register not available) Cleared by writing to register 0x0511.	r/(w)	r/(w)	0
14	Command error: 0: Last Command was successful 1: Invalid command or write command without Write Enable Cleared by executing a valid command or by writing “00” to Command register bits [9:8].	r/-	r/-	0
15	Busy: 0: MII Management Interface is idle 1: MII Management Interface is busy	r/-	r/-	0

NOTE: r/ (w): write access depends on assignment of MI (ECAT/PDI). Write access is blocked if Management interface is busy (0x0510[15]=1).

* Write enable bit 0 is self-clearing at the SOF of the next frame, Command bits [10:8] are self-clearing after the command is executed (Busy ends). Writing “00” to the command register will also clear the error bits [14:13]. The Command bits are cleared after the command is executed.

Table 72: Register PHY Address (0x0512)

	ESC20	ET1100	ET1200	IP Core
	~~[7]~~	~~[7]~~	~~[7]~~	[7] V3.0.0/ V3.00c

Bit	Description	ECAT	PDI	Reset Value
4:0	Target PHY Address Translation 0x0512[7]=0: 0-3: Target PHY Addresses 0-3 are used to access the PHYs at port 0-3, when the PHY addresses are properly configured 4-31: The configured PHY address of port 0 (PHY address offset) is added to the Target PHY Address values 4-31 when accessing a PHY Translation 0x0512[7]=1: 0-31: Target PHY Addresses is used when accessing a PHY without translation	r/(w)	r/(w)	0
6:5	Reserved, write 0	r/-	r/-	0
7	Target PHY Address translation: 0: Enabled 1: Disabled Refer to 0x0512[4:0] and 0x0510[7:3] for details.	r/(w)	r/(w)	0

NOTE: r/(w): write access depends on assignment of MI (ECAT/PDI). Write access is blocked if Management interface is busy (0x0510[15]=1).

Table 73: Register PHY Register Address (0x0513)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
4:0	Address of PHY Register that shall be read/written	r/(w)	r/(w)	0
7:5	Reserved, write 0	r/-	r/-	0

NOTE: r/(w): write access depends on assignment of MI (ECAT/PDI). Write access is blocked if Management interface is busy (0x0510[15]=1).

Table 74: Register PHY Data (0x0514:0x0515)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	PHY Read/Write Data	r/(w)	r/(w)	0

NOTE: r/(w): write access depends on assignment of MI (ECAT/PDI). Write access is blocked if Management interface is busy (0x0510[15]=1).

Table 75: Register MII Management ECAT Access State (0x0516)

ESC20	ET1100	ET1200	IP Core
			V2.0.0/ V2.00a

Bit	Description	ECAT	PDI	Reset Value
0	Access to MII management: 0: ECAT enables PDI takeover of MII management interface 1: ECAT claims exclusive access to MII management interface	r/(w)	r/-	0
7:1	Reserved, write 0	r/-	r/-	0

NOTE: r/(w): write access is only possible if 0x0517[0]=0.

Table 76: Register MII Management PDI Access State (0x0517)

ESC20	ET1100	ET1200	IP Core
			V2.0.0/ V2.00a

Bit	Description	ECAT	PDI	Reset Value
0	Access to MII management: 0: ECAT has access to MII management 1: PDI has access to MII management	r/-	r/(w)	0
1	Force PDI Access State: 0: Do not change Bit 0x0517[0] 1: Reset Bit 0x0517[0] to 0	r/w	r/-	0
7:2	Reserved, write 0	r/-	r/-	0

NOTE: r/(w): assigning access to PDI (bit 0 = 1) is only possible if 0x0516[0]=0 and 0x0517[1]=0. The SII EEPROM must be loaded (0x0110[0]=1) as well for IP Cores before V3.0.0/V3.00c.

Table 77: Register PHY Port y (port number y=0 to 3) Status (0x0518+y)

ESC20	ET1100	ET1200	IP Core
			V2.0.0/ V2.00a; [5] V2.0.2/ V2.02a

Bit	Description	ECAT	PDI	Reset Value
0	Physical link status (PHY status register 1.2): 0: No physical link 1: Physical link detected	r/-	r/-	0
1	Link status (100 Mbit/s, Full Duplex, Auto negotiation): 0: No link 1: Link detected	r/-	r/-	0
2	Link status error: 0: No error 1: Link error, link inhibited	r/-	r/-	0
3	Read error: 0: No read error occurred 1: A read error has occurred Cleared by writing any value to at least one of the PHY Port y Status registers.	r/(w/clr)	r/(w/clr)	0
4	Link partner error: 0: No error detected 1: Link partner error	r/-	r/-	0
5	PHY configuration updated: 0: No update 1: PHY configuration was updated Cleared by writing any value to at least one of the PHY Port y Status registers.	r/(w/clr)	r/(w/clr)	0
7:6	Reserved	r/-	r/-	0

NOTE: r/(w): write access depends on assignment of MI (ECAT/PDI).

2.47 FMMU (0x0600:0x06FF)

Each FMMU entry is described in 16 Bytes from 0x0600:0x060F to 0x06F0:0x06FF. Throughout this chapter, y is the FMMU index (y=0x0 to 0xF).

Table 78: FMMU Register overview

Register Address Offset	Length (Byte)	Description
+0x0:0x3	4	Logical Start Address
+0x4:0x5	2	Length
+0x6	1	Logical Start bit
+0x7	1	Logical Stop bit
+0x8:0x9	2	Physical Start Address
+0xA	1	Physical Start bit
+0xB	1	Type
+0xC	1	Activate
+0xD:0xF	3	Reserved

Table 79: Register Logical Start address FMMU y (0x06y0:0x06y3)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
31:0	Logical start address within the EtherCAT Address Space.	r/w	r/-	0	

Table 80: Register Length FMMU y (0x06y4:0x06y5)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
15:0	Offset from the first logical FMMU byte to the last FMMU byte + 1 (e.g., if two bytes are used, then this parameter shall contain 2)	r/w	r/-	0	

Table 81: Register Start bit FMMU y in logical address space (0x06y6)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
2:0	Logical starting bit that shall be mapped (bits are counted from least significant bit 0 to most significant bit 7)	r/w	r/-	0	
7:3	Reserved, write 0	r/-	r/-	0	

Table 82: Register Stop bit FMMU y in logical address space (0x06y7)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
2:0	Last logical bit that shall be mapped (bits are counted from least significant bit 0 to most significant bit 7)	r/w	r/-	0	
7:3	Reserved, write 0	r/-	r/-	0	

Table 83: Register Physical Start address FMMU y (0x06y8-0x06y9)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	Physical Start Address (mapped to logical Start address)	r/w	r/-	0

Table 84: Register Physical Start bit FMMU y (0x06yA)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
2:0	Physical starting bit as target of logical start bit mapping (bits are counted from least significant bit 0 to most significant bit 7)	r/w	r/-	0
7:3	Reserved, write 0	r/-	r/-	0

Table 85: Register Type FMMU y (0x06yB)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	0: Ignore mapping for read accesses 1: Use mapping for read accesses	r/w	r/-	0
1	0: Ignore mapping for write accesses 1: Use mapping for write accesses	r/w	r/-	0
7:2	Reserved, write 0	r/-	r/-	0

Table 86: Register Activate FMMU y (0x06yC)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	0: FMMU deactivated 1: FMMU activated. FMMU checks logically addressed blocks to be mapped according to configured mapping	r/w	r/-	0
7:1	Reserved, write 0	r/-	r/-	0

Table 87: Register Reserved FMMU y (0x06yD:0x06yF)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
23:0	Reserved, write 0	r/-	r/-	0

2.48 SyncManager (0x0800:0x087F)

SyncManager registers are mapped from 0x0800:0x0807 to 0x0878:0x087F. Throughout this chapter, y specifies SyncManager (y=0x0 to 0xF).

Table 88: SyncManager Register overview

Register Address Offset	Length (Byte)	Description
+0x0:0x1	2	Physical Start Address
+0x2:0x3	2	Length
+0x4	1	Control Register
+0x5	1	Status Register
+0x6	1	Activate
+0x7	1	PDI Control

Table 89: Register physical Start Address SyncManager y (0x0800+y*8:0x0801+y*8)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	First byte that will be handled by SyncManager	r/(w)	r/-	0

NOTE r/(w): Register can only be written if SyncManager is disabled (+0x6[0] = 0).

Table 90: Register Length SyncManager y (0x0802+y*8:0x0803+y*8)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	Number of bytes assigned to SyncManager (shall be greater than 1, otherwise SyncManager is not activated. If set to 1, only Watchdog Trigger is generated if configured)	r/(w)	r/-	0

NOTE r/(w): Register can only be written if SyncManager is disabled (+0x6[0] = 0).

Table 91: Register Control Register SyncManager y (0x0804+y*8)

	ESC20	ET1100	ET1200	IP Core
	~~[7]~~	~~[7]~~	~~[7]~~	~~[7]~~

Bit	Description	ECAT	PDI	Reset Value
1:0	Operation Mode: 00: Buffered (3 buffer mode) 01: Reserved 10: Mailbox (Single buffer mode) 11: Reserved	r/(w)	r/-	00
3:2	Direction: 00: Read: ECAT read access, PDI write access. 01: Write: ECAT write access, PDI read access. 10: Reserved 11: Reserved	r/(w)	r/-	00
4	Interrupt in ECAT Event Request Register: 0: Disabled 1: Enabled	r/(w)	r/-	0
5	Interrupt in AL Event Request Register: 0: Disabled 1: Enabled	r/(w)	r/-	0
6	Watchdog Trigger Enable: 0: Disabled 1: Enabled	r/(w)	r/-	0
7	Reserved, write 0	r/-	r/-	0

NOTE r/(w): Register can only be written if SyncManager is disabled (+0x6[0] = 0).

Table 92: Register Status Register SyncManager y (0x0805+y*8)

ESC20	ET1100	ET1200	IP Core
~~[2, 7:6]~~	~~[2, 7:6]~~	~~[2, 7:6]~~	~~[2]~~ [7:6] V2.3.0/ V2.03a

Bit	Description	ECAT	PDI	Reset Value
0	Interrupt Write: 1: Interrupt after buffer was completely and successfully written 0: Interrupt cleared after first byte of buffer was read NOTE: This interrupt is signalled to the reading side if enabled in the SM Control register.	r/-	r/-	0
1	Interrupt Read: 1: Interrupt after buffer was completely and successfully read 0: Interrupt cleared after first byte of buffer was written NOTE: This interrupt is signalled to the writing side if enabled in the SM Control register.	r/-	r/-	0
2	Reserved	r/-	r/-	0
3	Mailbox mode: mailbox status: 0: Mailbox empty 1: Mailbox full Buffered mode: reserved	r/-	r/-	0
5:4	Buffered mode: buffer status (last written buffer): 00: 1st buffer 01: 2nd buffer 10: 3rd buffer 11: (no buffer written) Mailbox mode: reserved	r/-	r/-	11
6	Read buffer in use (opened)	r/-	r/-	0
7	Write buffer in use (opened)	r/-	r/-	0

Table 93: Register Activate SyncManager y (0x0806+y*8)

ESC20	ET1100	ET1200	IP Core
~~[7:6] (w ack)~~	~~(w ack)~~	~~[7:6] (w ack)~~	

Bit	Description	ECAT	PDI	Reset Value
0	SyncManager Enable/Disable: 0: Disable: Access to Memory without SyncManager control 1: Enable: SyncManager is active and controls Memory area set in configuration	r/w	r/ (w ack)*	0
1	Repeat Request: A toggle of Repeat Request means that a mailbox retry is needed (primarily used in conjunction with ECAT Read Mailbox)	r/w	r/-	0
5:2	Reserved, write 0	r/-	r/-	0
6	Latch Event ECAT: 0: No 1: Generate Latch event when EtherCAT master issues a buffer exchange	r/w	r/-	0
7	Latch Event PDI: 0: No 1: Generate Latch events when PDI issues a buffer exchange or when PDI accesses buffer start address	r/w	r/-	0

* PDI register function acknowledge by Write command is disabled: Reading this register from PDI in all SyncManagers which have changed activation clears AL Event Request 0x0220[4]. Writing to this register from PDI is not possible.

PDI register function acknowledge by Write command is enabled: Writing register 0x0806 (SyncManager 0 only) from PDI clears AL Event Request 0x0220[4] for all SyncManagers. Writing to register 0x0806 (not 0x080E+y*8) from PDI is possible; write value is ignored (write 0).

Table 94: Register PDI Control SyncManager y (0x0807+y*8)

	ESC20	ET1100	ET1200	IP Core
	~~[7:6]~~	~~[7:6]~~	~~[7:6]~~	~~[7:6]~~

Bit	Description	ECAT	PDI	Reset Value
0	Deactivate SyncManager: Read: 0: Normal operation, SyncManager activated. 1: SyncManager deactivated and reset. SyncManager locks access to Memory area. Write: 0: Activate SyncManager 1: Request SyncManager deactivation NOTE: Writing 1 is delayed until the end of the frame, which is currently processed.	r/-	r/w	0
1	Repeat Ack: If this is set to the same value as that set by Repeat Request, the PDI acknowledges the execution of a previous set Repeat request.	r/-	r/w	0
7:2	Reserved, write 0	r/-	r/-	0

2.49 Distributed Clocks (0x0900:0x09FF)

2.49.1 Receive Times

Table 95: Register Receive Time Port 0 (0x0900:0x0903)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
7:0	Write: A write access to register 0x0900 with BWR or FPWR latches the local time at the beginning of the receive frame (start first bit of preamble) at each port. Write (ESC20, ET1200 exception): A write access latches the local time at the beginning of the receive frame at port 0. It enables the time stamping at the other ports. Read: Local time at the beginning of the last receive frame containing a write access to this register. NOTE: FPWR requires an address match for accessing this register like any FPWR command. All write commands with address match will increment the working counter (e.g., APWR), but they will not trigger receive time latching.	r/w (special function)	r/-	Undefined
31:8	Local time at the beginning of the last receive frame containing a write access to register 0x0900.	r/-	r/-	Undefined

NOTE: The time stamps cannot be read in the same frame in which this register was written.

Table 96: Register Receive Time Port 1 (0x0904:0x0907)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
31:0	Local time at the beginning of a frame (start first bit of preamble) received at port 1 containing a BWR or FPWR to register 0x0900. ESC20, ET1200 exception: Local time at the beginning of the first frame received at port 1 after time stamping was enabled. Time stamping is disabled for this port afterwards.	r/-	r/-	Undefined

Table 97: Register Receive Time Port 2 (0x0908:0x090B)

~~ESC20~~	ET1100	~~ET1200~~	IP Core

Bit	Description	ECAT	PDI	Reset Value
31:0	Local time at the beginning of a frame (start first bit of preamble) received at port 2 containing a BWR or FPWR to register 0x0900.	r/-	r/-	Undefined

Table 98: Register Receive Time Port 3 (0x090C:0x090F)

~~ESC20~~	ET1100	ET1200	~~IP Core~~

Bit	Description	ECAT	PDI	Reset Value
31:0	Local time at the beginning of a frame (start first bit of preamble) received at port 3 containing a BWR or FPWR to register 0x0900. ET1200 exception: Local time at the beginning of the first frame received at port 3 after time stamping was enabled. Time stamping is disabled for this port afterwards.	r/-	r/-	Undefined

NOTE: Register 0x0910:0x0913[0x910:0x0917] is described in the next chapter.

Table 99: Register Receive Time ECAT Processing Unit (0x0918:0x091F)

ESC20	ET1100	**ET1200**	IP Core
~~[63:32]~~			[63:32] config.

Bit	Description	ECAT	PDI	Reset Value
63:0	Local time at the beginning of a frame (start first bit of preamble) received at the ECAT Processing Unit containing a write access to register 0x0900 NOTE: E.g., if port 0 is open, this register reflects the Receive Time Port 0 as a 64 Bit value. Any valid EtherCAT write access to register 0x0900 triggers latching, not only BWR/FPWR commands as with register 0x0900.	r/-	r/-	Undefined

2.49.2 Time Loop Control Unit

Time Loop Control unit is usually assigned to ECAT. Write access to Time Loop Control registers by PDI instead of ECAT is only possible with explicit ESC configuration.

Table 100: Register System Time (0x0910:0x0913 [0x0910:0x0917])

ESC20	ET1100	**ET1200**	IP Core
~~[63:32]~~			[63:32] config.

Bit	Description	ECAT	PDI	Reset Value
63:0	ECAT read access: Local copy of the System Time when the frame passed the reference clock (i.e., including System Time Delay). Time latched at beginning of the frame (Ethernet SOF delimiter)	r	-	0
63:0	PDI read access: Local copy of the System Time. Time latched when reading first byte (0x0910)	-	r	
31:0	ECAT write access: Written value will be compared with the local copy of the System time. The result is an input to the time control loop. NOTE: written value will be compared at the end of the frame with the latched (SOF) local copy of the System time if at least the first byte (0x0910) was written.	(w) (special function)	-	
31:0	PDI write access: Written value will be compared with Latch0 Time Positive Edge time. The result is an input to the time control loop. NOTE: written value will be compared at the end of the access with Latch0 Time Positive Edge (0x09B0:0x09B3) if at least the last byte (0x0913) was written.	-	(w) (special function)	

NOTE: Write access to this register depends upon ESC configuration (System Time PDI-controlled off=ECAT/ on=PDI; ECAT control is common).

NOTE: Register 0x0918:0x091F is described in the previous chapter.

Table 101: Register System Time Offset (0x0920:0x0923 [0x0920:0x0927])

ESC20	ET1100	**ET1200**	IP Core
~~[63:32]~~			[63:32] config.

Bit	Description	ECAT	PDI	Reset Value
63:0	Difference between local time and System Time. Offset is added to the local time.	r/(w)	r/(w)	0

NOTE: Write access to this register depends upon ESC configuration (System Time PDI-controlled off=ECAT/ on=PDI; ECAT control is common). Reset internal system time difference filter and speed counter filter by writing Speed Counter Start (0x0930:0x0931) after changing this value.

Table 102: Register System Time Delay (0x0928:0x092B)

ESC20 ET1100 **ET1200** IP Core

Bit	Description	ECAT	PDI	Reset Value
31:0	Delay between Reference Clock and the ESC	r/(w)	r/(w)	0

NOTE: Write access to this register depends upon ESC configuration (System Time PDI-controlled off=ECAT/ on=PDI; ECAT control is common). Reset internal system time difference filter and speed counter filter by writing Speed Counter Start (0x0930:0x0931) after changing this value.

Table 103: Register System Time Difference (0x092C:0x092F)

ESC20 ET1100 **ET1200** IP Core

Bit	Description	ECAT	PDI	Reset Value
30:0	Mean difference between local copy of System Time and received System Time values *Difference = Received System Time – local copy of System Time*	r/-	r/-	0
31	0: Local copy of System Time less than received System Time 1: Local copy of System Time greater than or equal to received System Time	r/-	r/-	0

NOTE: Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

Table 104: Register Speed Counter Start (0x0930:0x931)

ESC20 ET1100 **ET1200** IP Core

Bit	Description	ECAT	PDI	Reset Value
14:0	Bandwidth for adjustment of local copy of System Time (larger values → smaller bandwidth and smoother adjustment) A write access resets System Time Difference (0x092C:0x092F) and Speed Counter Diff (0x0932:0x0933). Valid values: 0x0080 to 0x3FFF	r/(w)	r/(w)	0x1000
15	Reserved, write 0	r/-	r/-	0

NOTE: Write access to this register depends upon ESC configuration (System Time PDI-controlled off=ECAT/ on=PDI; ECAT control is common).

Table 105: Register Speed Counter Diff (0x0932:0x933)

ESC20 ET1100 **ET1200** IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	Representation of the deviation between local clock period and Reference Clock's clock period (representation: two's complement) Range: ±(Speed Counter Start – 0x7F)	r/-	r/-	0x0000

NOTE: Calculate the clock deviation after System Time Difference has settled at a low value as follows:

$$\text{Deviation} = \frac{\text{Speed Counter Diff}}{5\,(\text{Speed Counter Start} + \text{Speed Counter Diff} + 2)(\text{Speed Counter Start} - \text{Speed Counter Diff} + 2)}$$

$$\text{Local clock period} = (1 - \text{Deviation}) * \text{Reference clock period}$$

Table 106: Register System Time Difference Filter Depth (0x0934)

ESC20 ET1100 **ET1200** IP Core

Bit	Description	ECAT	PDI	Reset Value
3:0	Filter depth for averaging the received System Time deviation IP Core since V2.2.0/V2.02a: A write access resets System Time Difference (0x092C:0x092F)	r/(w)	r/(w)	4
7:4	Reserved, write 0	r/-	r/-	0

NOTE: Write access to this register depends upon ESC configuration (System Time PDI-controlled off=ECAT/ on=PDI; ECAT control is common).
ET1100, ET1200, ESC20, IP Core before V2.2.0/V2.02a: Reset System Time Difference by writing Speed Counter Start (0x0930:0x0931) after changing this value.

Table 107: Register Speed Counter Filter Depth (0x0935)

ESC20 ET1100 **ET1200** IP Core

Bit	Description	ECAT	PDI	Reset Value
3:0	Filter depth for averaging the clock period deviation IP Core since V2.2.0/V2.02a: A write access resets the internal speed counter filter.	r/(w)	r/(w)	12
7:4	Reserved, write 0	r/-	r/-	0

NOTE: Write access to this register depends upon ESC configuration (System Time PDI-controlled off=ECAT/ on=PDI; ECAT control is common).
ET1100, ET1200, ESC20, IP Core before V2.2.0/V2.02a: Reset internal speed counter filter by writing Speed Counter Start (0x0930:0x0931) after changing this value.

Table 108: Register Receive Time Latch Mode (0x0936)

~~ESC20~~ ~~ET1100~~ **ET1200** ~~IP Core~~

Bit	Description	ECAT	PDI	Reset Value
0	Receive Time Latch Mode: 0: Forwarding mode (used if frames are entering the ESC at port 0 first): Receive time stamps of ports 1-3 are enabled after the write access to 0x0900, so the following frame at ports 1-3 will be time stamped (this is typically the write frame to 0x0900 coming back from the network behind the ESC). 1: Reverse mode (used if frames are entering ESC at port 1-3 first): Receive time stamps of ports 1-3 are immediately taken over from the internal hidden time stamp registers, so the previous frame entering the ESC at ports 1-3 will be time stamped when the write frame to 0x0900 enters port 0 (the previous frame at ports 1-3 is typically the write frame to 0x0900 coming from the master, which will enable time stamping at the ESC once it enters port 0).	r/w	r/-	0
7:1	Reserved	r/-	r/-	0

NOTE: There should not be frames traveling around the network before and after the time stamps are taken, otherwise these frames might get time-stamped and not the write frame to 0x0900.

2.49.3 Cyclic Unit Control

Table 109: Register Cyclic Unit Control (0x0980)

ESC20	ET1100	**ET1200**	IP Core
~~[3:1, 7:6]~~	~~[3:1, 7:6]~~	~~[3:1, 7:6]~~	~~[3:1, 7:6]~~

Bit	Description	ECAT	PDI	Reset Value
0	Cyclic Unit and SYNC0 out unit control: 0: ECAT-controlled 1: PDI-controlled	r/w	r/-	0
3:1	Reserved, write 0	r/-	r/-	0
4	Latch In unit 0: 0: ECAT-controlled 1: PDI-controlled NOTE: Latch interrupt is routed to ECAT/PDI depending on this setting. Always 1 (PDI-controlled) if System Time is PDI-controlled.	r/w	r/-	0
5	Latch In unit 1: 0: ECAT-controlled 1: PDI-controlled NOTE: Latch interrupt is routed to ECAT/PDI depending on this setting	r/w	r/-	0
7:6	Reserved, write 0	r/-	r/-	0

2.49.4 SYNC Out Unit

Table 110: Register Activation register (0x0981)

ESC20	ET1100	ET1200	IP Core
~~[7:3]~~	~~[7:3]~~	~~[7:3]~~	[7:3] V2.2.0/ V2.02a

Bit	Description	ECAT	PDI	Reset Value
0	Sync Out Unit activation: 0: Deactivated 1: Activated	r/(w)	r/(w)	0
1	SYNC0 generation: 0: Deactivated 1: SYNC0 pulse is generated	r/(w)	r/(w)	0
2	SYNC1 generation: 0: Deactivated 1: SYNC1 pulse is generated	r/(w)	r/(w)	0
3	Auto-activation by writing Start Time Cyclic Operation (0x0990:0x0997): 0: Disabled 1: Auto-activation enabled. 0x0981[0] is set automatically after Start Time is written.	r/(w)	r/(w)	0
4	Extension of Start Time Cyclic Operation (0x0990:0x0993): 0: No extension 1: Extend 32 bit written Start Time to 64 bit	r/(w)	r/(w)	0
5	Start Time plausibility check: 0: Disabled. SyncSignal generation if Start Time is reached. 1: Immediate SyncSignal generation if Start Time is outside near future (see 0x0981[6])	r/(w)	r/(w)	0
6	Near future configuration (approx.): 0: ½ DC width future (2^{31} ns or 2^{63} ns) 1: ~2.1 sec. future (2^{31} ns)	r/(w)	r/(w)	0
7	SyncSignal debug pulse (Vasily bit): 0: Deactivated 1: Immediately generate one ping only on SYNC0-1 according to 0x0981[2:1 for debugging This bit is self-clearing, always read 0. All pulses are generated at the same time, the cycle time is ignored. The configured pulse length is used.	r/(w)	r/(w)	0

NOTE: Write to this register depends upon setting of 0x0980[0]

Table 111: Register Pulse Length of SyncSignals (0x0982:0x983)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
15:0	Pulse length of SyncSignals (in Units of 10ns) 0: Acknowledge mode: SyncSignal will be cleared by reading SYNC[1:0] Status register	r/-	r/-	IP Core: Depends on configuration Others: 0, later EEPROM word 2

Table 112: Register Activation Status (0x0984)

~~ESC20~~	~~ET1100~~	~~ET1200~~	IP Core
			V2.2.0/ V2.02a ~~[7:3]~~

Bit	Description	ECAT	PDI	Reset Value
0	SYNC0 activation state: 0: First SYNC0 pulse is not pending 1: First SYNC0 pulse is pending	r/-	r/-	0
1	SYNC1 activation state: 0: First SYNC1 pulse is not pending 1: First SYNC1 pulse is pending	r/-	r/-	0
2	Start Time Cyclic Operation (0x0990:0x0997) plausibility check result when Sync Out Unit was activated: 0: Start Time was within near future 1: Start Time was out of near future (0x0981[6])	r/-	r/-	0
7:3	Reserved	r/-	r/-	0

Table 113: Register SYNC0 Status (0x098E)

ESC20 (w ack)	ET1100 (w ack)	ET1200 (w ack)	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	SYNC0 state for Acknowledge mode. SYNC0 in Acknowledge mode is cleared by reading this register from PDI, use only in Acknowledge mode	r/-	r/ (w ack)*	0
7:1	Reserved	r/-	r/ (w ack)*	0

* PDI register function acknowledge by Write command is disabled: Reading this register from PDI clears AL Event Request 0x0220[2]. Writing to this register from PDI is not possible.
PDI register function acknowledge by Write command is enabled: Writing this register from PDI clears AL Event Request 0x0220[2]. Writing to this register from PDI is possible; write value is ignored (write 0).

Table 114: Register SYNC1 Status (0x098F)

ESC20 (w ack)	ET1100 (w ack)	ET1200 (w ack)	IP Core

Bit	Description	ECAT	PDI	Reset Value
0	SYNC1 state for Acknowledge mode. SYNC1 in Acknowledge mode is cleared by reading this register from PDI, use only in Acknowledge mode	r/-	r/ (w ack)*	0
7:1	Reserved	r/-	r/ (w ack)*	0

* PDI register function acknowledge by Write command is disabled: Reading this register from PDI clears AL Event Request 0x0220[3]. Writing to this register from PDI is not possible.
PDI register function acknowledge by Write command is enabled: Writing this register from PDI clears AL Event Request 0x0220[3]. Writing to this register from PDI is possible; write value is ignored (write 0).

Table 115: Register Start Time Cyclic Operation (0x0990:0x0993 [0x0990:0x0997])

ESC20	ET1100	ET1200	IP Core
~~[63:32]~~			[63:32] config.

Bit	Description	ECAT	PDI	Reset Value
63:0	Write: Start time (System time) of cyclic operation in ns Read: System time of next SYNC0 pulse in ns	r/(w)	r/(w)	0

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.
Write to this register depends upon setting of 0x0980[0].

Extension of Start Time (0x0981[4]=1): upper 32 bits are automatically extended after writing the lower 32 bits only. Upper 32 bits are taken from current System Time.

Explicit activation (0x0981[3]=0): Register value is used when 0x0981[0] has a transition to 1.
Auto-activation (0x0981[3]=1): a) 32 Bit Distributed Clocks or Extension of Start Time used (0x0981[4]=1): 0x0981[0] is set automatically after 0x0993 is written.
b) 64 Bit Distributed Clocks: 0x0981[0] is set automatically after 0x0997 is written

Table 116: Register Next SYNC1 Pulse (0x0998:0x099B [0x0998:0x099F])

ESC20	ET1100	ET1200	IP Core
~~[63:32]~~			[63:32] config.

Bit	Description	ECAT	PDI	Reset Value
63:0	System time of next SYNC1 pulse in ns	r/-	r/-	0

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

Table 117: Register SYNC0 Cycle Time (0x09A0:0x09A3)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
31:0	Time between two consecutive SYNC0 pulses in ns. 0: Single shot mode, generate only one SYNC0 pulse.	r/(w)	r/(w)	0

NOTE: Write to this register depends upon setting of 0x0980[0]. Minimum value for cyclic operation: 60 [ns].

Table 118: Register SYNC1 Cycle Time (0x09A4:0x09A7)

ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
31:0	Time between SYNC0 pulse and SYNC1 pulse in ns	r/(w)	r/(w)	0

NOTE: Write to this register depends upon setting of 0x0980[0].

2.49.5 Latch In unit

Table 119: Register Latch0 Control (0x09A8)

ESC20 ET1100 **ET1200** IP Core

Bit	Description	ECAT	PDI	Reset Value
0	Latch0 positive edge: 0: Continuous Latch active 1: Single event (only first event active)	r/(w)	r/(w)	0
1	Latch0 negative edge: 0: Continuous Latch active 1: Single event (only first event active)	r/(w)	r/(w)	0
7:2	Reserved, write 0	r/-	r/-	0

NOTE: Write access depends upon setting of 0x0980[4].

Table 120: Register Latch1 Control (0x09A9)

ESC20 ET1100 **ET1200** IP Core

Bit	Description	ECAT	PDI	Reset Value
0	Latch1 positive edge: 0: Continuous Latch active 1: Single event (only first event active)	r/(w)	r/(w)	0
1	Latch1 negative edge: 0: Continuous Latch active 1: Single event (only first event active)	r/(w)	r/(w)	0
7:2	Reserved, write 0	r/-	r/-	0

NOTE: Write access depends upon setting of 0x0980[5].

Table 121: Register Latch0 Status (0x09AE)

	ESC20	ET1100	ET1200	IP Core
	[2]		[2]	

Bit	Description	ECAT	PDI	Reset Value
0	Event Latch0 positive edge. 0: Positive edge not detected or continuous mode 1: Positive edge detected in single event mode only. Flag cleared by reading out Latch0 Time Positive Edge.	r/-	r/-	0
1	Event Latch0 negative edge. 0: Negative edge not detected or continuous mode 1: Negative edge detected in single event mode only. Flag cleared by reading out Latch0 Time Negative Edge.	r/-	r/-	0
2	Latch0 pin state	r/-	r/-	0
7:3	Reserved	r/-	r/-	0

Table 122: Register Latch1 Status (0x09AF)

	ESC20	ET1100	ET1200	IP Core
	[2]		[2]	

Bit	Description	ECAT	PDI	Reset Value
0	Event Latch1 positive edge. 0: Positive edge not detected or continuous mode 1: Positive edge detected in single event mode only. Flag cleared by reading out Latch1 Time Positive Edge.	r/-	r/-	0
1	Event Latch1 negative edge. 0: Negative edge not detected or continuous mode 1: Negative edge detected in single event mode only. Flag cleared by reading out Latch1 Time Negative Edge.	r/-	r/-	0
2	Latch1 pin state	r/-	r/-	0
7:3	Reserved	r/-	r/-	0

Table 123: Register Latch0 Time Positive Edge (0x09B0:0x09B3 [0x09B0:0x09B7])

ESC20	ET1100	ET1200	IP Core
~~[63:32 (w ack)]~~	~~(w ack)~~	~~(w ack)~~	[63:32] config.

Bit	Description	ECAT	PDI	Reset Value
63:0	System time at the positive edge of the Latch0 signal.	r(ack)/-	r/ (w ack)*	0

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value. Reading this register from ECAT clears Latch0 Status 0x09AE[0] if 0x0980[4]=0. Writing to this register from ECAT is not possible.

* PDI register function acknowledge by Write command is disabled: Reading this register from PDI if 0x0980[4]=1 clears Latch0 Status 0x09AE[0]. Writing to this register from PDI is not possible.
PDI register function acknowledge by Write command is enabled: Writing this register from PDI if 0x0980[4]=1 clears Latch0 Status 0x09AE[0]. Writing to this register from PDI is possible; write value is ignored (write 0).

Table 124: Register Latch0 Time Negative Edge (0x09B8:0x09BB [0x09B8:0x09BF])

ESC20	ET1100	ET1200	IP Core
~~[63:32] (w ack)~~	~~(w ack)~~	~~(w ack)~~	[63:32] config.

Bit	Description	ECAT	PDI	Reset Value
63:0	System time at the negative edge of the Latch0 signal.	r(ack)/-	r/ (w ack)*	0

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value. Reading this register from ECAT clears Latch0 Status 0x09AE[1] if 0x0980[4]=0. Writing to this register from ECAT is not possible.

* PDI register function acknowledge by Write command is disabled: Reading this register from PDI if 0x0980[4]=1 clears Latch0 Status 0x09AE[1]. Writing to this register from PDI is not possible.
PDI register function acknowledge by Write command is enabled: Writing this register from PDI if 0x0980[4]=1 clears Latch0 Status 0x09AE[1]. Writing to this register from PDI is possible; write value is ignored (write 0).

Table 125: Register Latch1 Time Positive Edge (0x09C0:0x09C3 [0x09C0:0x09C7])

ESC20	ET1100	ET1200	IP Core
~~[63:32] (w ack)~~	~~(w ack)~~	~~(w ack)~~	[63:32] config.

Bit	Description	ECAT	PDI	Reset Value
63:0	System time at the positive edge of the Latch1 signal.	r(ack)/-	r/ (w ack)*	0

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value. Reading this register from ECAT clears Latch0 Status 0x09AF[0] if 0x0980[5]=0. Writing to this register from ECAT is not possible.

* PDI register function acknowledge by Write command is disabled: Reading this register from PDI if 0x0980[5]=1 clears Latch0 Status 0x09AF[0]. Writing to this register from PDI is not possible.
PDI register function acknowledge by Write command is enabled: Writing this register from PDI if 0x0980[5]=1 clears Latch0 Status 0x09AF[0]. Writing to this register from PDI is possible; write value is ignored (write 0).

Table 126: Register Latch1 Time Negative Edge (0x09C8:0x09CB [0x09C8:0x09CF])

ESC20	ET1100	ET1200	IP Core
~~[63:32] (w ack)~~	~~(w ack)~~	~~(w ack)~~	[63:32] config.

Bit	Description	ECAT	PDI	Reset Value
63:0	System time at the negative edge of the Latch1 signal.	r(ack)/-	r/ (w ack)*	0

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value. Reading this register from ECAT clears Latch0 Status 0x09AF[1] if 0x0980[5]=0. Writing to this register from ECAT is not possible.

* PDI register function acknowledge by Write command is disabled: Reading this register from PDI if 0x0980[5]=1 clears Latch0 Status 0x09AF[1]. Writing to this register from PDI is not possible.
PDI register function acknowledge by Write command is enabled: Writing this register from PDI if 0x0980[5]=1 clears Latch0 Status 0x09AF[1]. Writing to this register from PDI is possible; write value is ignored (write 0).

2.49.6 SyncManager Event Times

Table 127: Register EtherCAT Buffer Change Event Time (0x09F0:0x09F3)

~~ESC20~~ ET1100 ~~ET1200~~ IP Core

Bit	Description	ECAT	PDI	Reset Value
31:0	Local time at the beginning of the frame which causes at least one SyncManager to assert an ECAT event	r/-	r/-	0

NOTE: Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

Table 128: Register PDI Buffer Start Event Time (0x09F8:0x09FB)

~~ESC20~~ ET1100 ~~ET1200~~ IP Core

Bit	Description	ECAT	PDI	Reset Value
31:0	Local time when at least one SyncManager asserts a PDI buffer start event	r/-	r/-	0

NOTE: Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

Table 129: Register PDI Buffer Change Event Time (0x09FC:0x09FF)

~~ESC20~~ ET1100 ~~ET1200~~ IP Core

Bit	Description	ECAT	PDI	Reset Value
31:0	Local time when at least one SyncManager asserts a PDI buffer change event	r/-	r/-	0

NOTE: Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

2.50 ESC-specific registers (0x0E00:0x0EFF)

2.50.1 ET1200

Table 130: Register Power-On Values ET1200 (0x0E00)

~~ESC20~~ ~~ET1100~~ **ET1200** ~~IP Core~~

Bit	Description	ECAT	PDI	Reset Value
1:0	Chip mode (MODE): 00: Port 0: EBUS, Port 1: EBUS, 18 pin PDI 01: Reserved 10: Port 0: MII, Port 1: EBUS, 8 pin PDI 11: Port 0: EBUS, Port 1: MII, 8 pin PDI	r/-	r/-	Depends on Hardware configuration
3:2	CPU clock output (CLK_MODE): 00: Off – PDI[7] available as PDI port 01: PDI[7] = 25MHz 10: PDI[7] = 20MHz 11: PDI[7] = 10MHz	r/-	r/-	
5:4	TX signal shift (C25_SHI): 00: MII TX signals shifted by 0° 01: MII TX signals shifted by 90° 10: MII TX signals shifted by 180° 11: MII TX signals shifted by 270°	r/-	r/-	
6	CLK25 Output Enable (C25_ENA): 0: Disabled – PDI[6] available as PDI port 1: Enabled – PDI[6] = 25MHz (OSC) NOTE: Only used in Chip mode 10 and 11	r/-	r/-	
7	PHY Address Offset (PHYAD_OFF): 0: No PHY address offset 1: PHY address offset is 16	r/-	r/-	

2.50.2 ET1100

Table 131: Register Power-On Values ET1100 (0x0E00:0x0E01)

~~ESC20~~ **ET1100** ~~ET1200~~ ~~IP Core~~

Bit	Description	ECAT	PDI	Reset Value
1:0	Port mode (P_MODE): 00: Logical ports 0 and 1 available 01: Logical ports 0, 1 and 2 available 10: Logical ports 0, 1 and 3 available 11: Logical ports 0, 1, 2 and 3 available	r/-	r/-	Depends on Hardware configuration
5:2	Physical layer of available ports (P_CONF). Bit 2 → logical port 0, Bit 3 → logical port 1, Bit 4 → third logical port (2/3), Bit 5 → logical port 3. 0: EBUS 1: MII	r/-	r/-	
7:6	CPU clock output (CLK_MODE): 00: Off – PDI[7] available as PDI port 01: PDI[7] = 25MHz 10: PDI[7] = 20MHz 11: PDI[7] = 10MHz	r/-	r/-	
9:8	TX signal shift (C25_SHI): 00: MII TX signals shifted by 0° 01: MII TX signals shifted by 90° 10: MII TX signals shifted by 180° 11: MII TX signals shifted by 270°	r/-	r/-	
10	CLK25 Output Enable (C25_ENA): 0: Disabled – PDI[31] available as PDI port 1: Enabled – PDI[31] = 25MHz (OSC)	r/-	r/-	
11	Transparent Mode MII (Trans_Mode_Ena): 0: Disabled 1: Enabled – ERR is input (0: TX signals are tri-stated, 1: ESC is driving TX signals)	r/-	r/-	
12	Digital Control/State Move (Ctrl_Status_Move): 0: Control/Status signals are mapped to PDI[39:32] – if available 1: Control/Status signals are remapped to the highest available PDI Byte.	r/-	r/-	
13	PHY Address Offset (PHYAD_OFF): 0: No PHY address offset 1: PHY address offset is 16	r/-	r/-	
14	PHY Link Polarity (LINKPOL): 0: LINK_MII is active low 1: LINK_MII is active high	r/-	r/-	
15	Reserved configuration bit	r/-	r/-	

2.50.3 IP Core

Table 132: Register Product ID IP Core (0x0E00:0x0E07)

~~ESC20~~ ~~ET1100~~ ~~ET1200~~ **IP Core**

Bit	Description	ECAT	PDI	Reset Value
63:0	Product ID	r/-	r/-	Depends on configuration

Table 133: Register Vendor ID IP Core (0x0E08:0x0E0F)

~~ESC20~~ ~~ET1100~~ ~~ET1200~~ **IP Core**

Bit	Description	ECAT	PDI	Reset Value
31:0	Vendor ID: [23:0] Company [31:24] Department NOTE: Test Vendor IDs have [31:28]=0xE	r/-	r/-	Depends on License file/signed Vendor ID
63:32	Reserved	r/-	r/-	

2.50.4 ESC20

Table 134: Register FPGA Update (0x0E00:0x0EFF)

	ESC20	~~ET1100~~	~~ET1200~~	~~IP Core~~

Bit	Description	ECAT	PDI	Reset Value
---	FPGA Update (ESC20 and TwinCAT only)			

2.51 Digital I/O Output Data (0x0F00:0x0F03)

Table 135: Register Digital I/O Output Data (0x0F00:0x0F03)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
31:0	Output Data	r/w	r/-	0	

NOTE: Register size depends on PDI setting and/or device configuration. This register is bit-writable (using Logical addressing).

2.52 General Purpose Outputs (0x0F10:0x0F17)

Table 136: Register General Purpose Outputs (0x0F10:0x0F17)

		~~ESC20~~	ET1100	ET1200	IP Core
			~~[63:16]~~ config.	~~[63:12]~~	config
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
7:0 15:0 31:0 63:0	General Purpose Output Data	r/w	r/w	0	

NOTE: Register size depends on PDI setting and/or device configuration

2.53 General Purpose Inputs (0x0F18:0x0F1F)

Table 137: Register General Purpose Inputs (0x0F18:0x0F1F)

		~~ESC20~~	ET1100	~~ET1200~~	IP Core
			~~[63:16]~~ config.		config
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
7:0 15:0 31:0 63:0	General Purpose Input Data	r/-	r/-	0	

NOTE: Register size depends on PDI setting and/or device configuration

2.54 User RAM (0x0F80:0x0FFF)

Table 138: User RAM (0x0F80:0x0FFF)

		ESC20	ET1100	ET1200	IP Core
Bit	**Description**	**ECAT**	**PDI**	**Reset Value**	
----	Application-specific information	r/w	r/w	IP Core: Extended ESC features Others: Random/undefined	

Table 139: Extended ESC Features (power-on values of User RAM)

				~~ESC20~~	~~ET1100~~	~~ET1200~~	**IP Core**
							V1.1.0/ V1.01a
Addr.	**Bit**	**Feat.**	**Description**	**Reset Value IP Core**			
			ESC Features				
0F80	7:0	-	Number of extended feature bits	Depends on ESC Intel: V1.1.0-V1.1.1 31 V2.00 35 V2.2.0-V2.2.1 41 V2.3.0-V2.3.1 49 V2.4.0 51 V2.4.3-V2.4.4 142 V3.0.0 149 V3.0.1-V3.0.10 150 Xilinx: V1.01a 31 V2.00a 35 V2.02a 41 V2.03a-V2.03d 49 V2.04a 51 V2.04d-V2.04e 142 V3.00c-V3.00k 150			

Addr.	Bit	Feat.	Description	Reset Value IP Core
			ESC extended features:	Depends on ESC: 0: Not available 1: Available c: Configurable
0F81	0	0	Extended DL Control Register (0x0102:0x0103)	1
	1	1	AL Status Code Register (0x0134:0x0135)	c
	2	2	ECAT Interrupt Mask (0x0200:0x0201)	1
	3	3	Configured Station Alias (0x0012:0x0013)	1
	4	4	General Purpose Inputs (0x0F18:0x0F1F)	c
	5	5	General Purpose Outputs (0x0F10:0x0F17)	c
	6	6	AL Event Mask writable (0x0204:0x0207)	c
	7	7	Physical Read/Write Offset (0x0108:0x0109)	c
0F82	0	8	Watchdog divider writable (0x0400:0x0401) and Watchdog PDI (0x0410:0x0411)	c
	1	9	Watchdog counters (0x0442:0x0443)	c
	2	10	Write Protection (0x0020:0x0031)	c
	3	11	Reset (0x0040:0x0041)	c
	4	12	Reserved	0
	5	13	DC SyncManager Event Times (0x09F0:0x09FF)	c
	6	14	ECAT Processing Unit/PDI Error Counter (0x030C:0x030D)	c
	7	15	EEPROM Size configurable (0x0502[7]): 0: EEPROM Size fixed to sizes up to 16 Kbit 1: EEPROM Size configurable	1
0F83	0	16	Reserved	0 1 since V3.0.0
	1	17	Reserved	0
	2	18	Reserved	0
	3	19	Lost Link Counter (0x0310:0x0313)	c
	4	20	MII Management Interface (0x0510:0x0515)	c
	5	21	Enhanced Link Detection MII	c
	6	22	Enhanced Link Detection EBUS	0
	7	23	Run LED (DEV_STATE LED)	c
0F84	0	24	Link/Activity LED	1
	1	25	Reserved	0
	2	26	Reserved	1
	3	27	DC Latch In Unit	c
	4	28	Reserved	0
	5	29	DC Sync Out Unit	c
	6	30	DC Time loop control assigned to PDI	c
	7	31	Link detection and configuration by MI	c

Addr.	Bit	Feat.	Description	Reset Value IP Core
0F85	0	32	MI control by PDI possible	1
	1	33	Automatic TX shift	c
	2	34	EEPROM emulation by µController	c
	3	35	Reserved	0
	4	36	Reserved	0
	5	37	Disable Digital I/O register (0x0F00:0x0F03)	c
	6	38	Reserved	0
	7	39	Reserved	0
0F86	0	40	Reserved	0
	1	41	Reserved	0
	2	42	RUN/ERR LED Override (0x0138:0x0139)	c
	3	43	Reserved	0
	4	44	Reserved	1
	5	45	Reserved	0
	6	46	Reserved	0
	7	47	Reserved	0
0F87	0	48	Reserved	0
	1	49	Reserved	0
	2	50	Reserved	0
	3	51	DC Sync1 disable	c
	4	52	Reserved	0
	5	53	Reserved	0
	6	54	DC Receive Times (0x0900:0x090F)	c
	7	55	DC System Time (0x0910:0x0936)	c
0F88	0	56	DC 64 bit	c
	1	57	Reserved	0
	2	58	PDI clears error counter	0
	3	59	Avalon PDI	c
	4	60	OPB PDI	0
	5	61	PLB PDI	c
	6	62	Reserved	0
	7	63	Reserved	0
0F89	0	64	Reserved	0
	1	65	Reserved	0
	2	66	Reserved	0
	3	67	Reserved	0
	4	68	Reserved	0
	5	69	Reserved	0
	6	70	Reserved	0
	7	71	Direct RESET	0

Addr.	Bit	Feat.	Description	Reset Value IP Core
0F8A	0	72	Reserved	0
	1	73	Reserved	1
	2	74	DC Latch1 disable	c
	3	75	AXI PDI	c
	4	76	Reserved	0
	5	77	Reserved	0
	6	78	PDI function acknowledge by PDI write	c
	7	79	PDI Information register (0x014E:0x014F)	c
0F8B	0	80	Reserved	1
	1	81	Reserved	1
	2	82	Reserved	0
	3	83	LED test	c
	4	84	Reserved	0
	5	85	Reserved	0
	6	86	Reserved	0
	7	87	Reserved	0
0F8C	3:0	91:88	Reserved	0
	7:4	95:92	Reserved	0
0F8D	3:0	99:96	Reserved	0
	7:4	103:100	Reserved	0
0F8E	3:0	107:104	Reserved	0
	4	108	Reserved	0
	5	109	Reserved	0
	7:6	112:110	Digital I/O PDI byte size	c
0F8F	0			
	1	113	Reserved	0
	2	114	Digital I/O PDI	c
	3	115	SPI Slave PDI	c
	4	116	Asynchronous µC PDI	c
	5	117	Reserved	0
	6	118	Reserved	1
	7	119	Reserved	1

Addr.	Bit	Feat.	Description	Reset Value IP Core
0F90	0	120	Reserved	0
	1	121	Reserved	0
	2	122	Reserved	0
	3	123	Reserved	0
	4	124	Reserved	0
	5	125	Reserved	0
	6	126	Reserved	0
	7	127	Reserved	0
0F91	0	128	Reserved	0
	1	129	Reserved	0
	2	130	Reserved	0
	3	131	Reserved	0
	4	132	Reserved	0
	5	133	Reserved	0
	6	134	Reserved	0
	7	135	Reserved	0
0F92	0	136	Reserved	0
	1	137	Reserved	0
	2	138	Reserved	0
	3	139	Reserved	0
	4	140	Reserved	0
	5	141	Reserved	0
	6	142	Reserved	0
	7	143	Reserved	0
0F93	0	144	RGMII	c
	1	145	Individual PHY address read out (0x0510[7:3])	c
	2	146	CLK_PDI_EXT is asynchronous	c
	3	147	Reserved	0
	4	148	Use RGMII GTX_CLK phase shifted clock input	1
	5	149	RMII	c
	6	150	Security CPLD protection	0
	7	153:151	Reserved	0
0F94	1:0			
	5:2	157:154	Reserved	0
	6	158	Reserved	0
	7	159	Reserved	0

Addr.	Bit	Feat.	Description	Reset Value IP Core
0F95 - 0FFF	7:0		Reserved	0

NOTE: Reset values are for IP Core V3.00k/V3.0.10

3 Process Data RAM (0x1000:0xFFFF)

3.1 PDI Digital I/O Input Data (0x1000:0x1003)

Digital I/O Input Data is written into the Process Data RAM by the Digital I/O PDI.

Table 140: Digital I/O Input Data (0x1000:0x1003)

	ESC20	ET1100	ET1200	IP Core

Bit	Description	ECAT	PDI	Reset Value
31:0	Input Data	(r/w)	(r/w)	Random/undefined

NOTE: (r/w) Process Data RAM is only accessible if EEPROM was correctly loaded (register 0x0110[0] = 1).

NOTE: Input Data size depends on PDI setting and/or device configuration. Digital I/O Input Data is written into the Process Data RAM at these addresses if a Digital I/O PDI with inputs is configured.

3.2 Process Data RAM (0x1000:0xFFFF)

The Process Data RAM starts at address 0x1000, its size depends on the ESC.

Table 141: Process Data RAM (0x1000:0xFFFF)

	ESC20	ET1100	ET1200	IP Core
	4 Kbyte	8 Kbyte	1 Kbyte	config.

Bit	Description	ECAT	PDI	Reset Value
	Process Data RAM	(r/w)	(r/w)	Random/undefined

NOTE: (r/w) Process Data RAM is only accessible if EEPROM was correctly loaded (register 0x0110[0] = 1).

4 Appendix

4.1 Support and Service

Beckhoff and our partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

4.1.1 Beckhoff's branch offices and representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products!

The addresses of Beckhoff's branch offices and representatives round the world can be found on her internet pages: http://www.beckhoff.com

You will also find further documentation for Beckhoff components there.

4.2 Beckhoff Headquarters

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Web: www.beckhoff.com

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