Application note

EtherCAT® Slave Controller

Section I – Technology
(Online at http://www.beckhoff.com)

Section II – Register description
(Online at http://www.beckhoff.com)

Section III – Hardware description
(Online at http://www.beckhoff.com)

Application note – PHY selection guide

Requirements to Ethernet PHYs used for EtherCAT and EtherCAT G
Ethernet PHY Examples

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BECKHOFF

DOCUMENT ORGANIZATION

The Beckhoff EtherCAT Slave Controller (ESC) documentation covers the following Beckhoff ESCs:

- ET1200
- ET1100
- EtherCAT IP Core for Altera® FPGAs
- EtherCAT IP Core for AMD®(Xilinx®) FPGAs
- ESC20

The documentation is organized in three sections. Section I and section II are common for all Beckhoff ESCs, Section III is specific for each ESC variant.

The latest documentation is available at the Beckhoff homepage (http://www.beckhoff.com).

Section I – Technology (All ESCs)

Section I deals with the basic EtherCAT technology. Starting with the EtherCAT protocol itself, the frame processing inside EtherCAT slaves is described. The features and interfaces of the physical layer with its two alternatives Ethernet and EBUS are explained afterwards. Finally, the details of the functional units of an ESC like FMMU, SyncManager, Distributed Clocks, Slave Information Interface, Interrupts, Watchdogs, and so on, are described.

Since Section I is common for all Beckhoff ESCs, it might describe features which are not available in a specific ESC. Refer to the feature details overview in Section III of a specific ESC to find out which features are available.

Section II – Register Description (All ESCs)

Section II contains detailed information about all ESC registers. This section is also common for all Beckhoff ESCs, thus registers, register bits, or features are described which might not be available in a specific ESC. Refer to the register overview and to the feature details overview in Section III of a specific ESC to find out which registers and features are available.

Section III – Hardware Description (Specific ESC)

Section III is ESC specific and contains detailed information about the ESC features, implemented registers, configuration, interfaces, pinout, usage, electrical and mechanical specification, and so on. Especially the Process Data Interfaces (PDI) supported by the ESC are part of this section.

Additional Documentation

Application notes and utilities can also be found at the Beckhoff homepage. Pinout configuration tools for ET1100/ET1200 are available. Additional information on EtherCAT IP Cores with latest updates regarding design flow compatibility, FPGA device support and known issues are also available.

DOCUMENT HISTORY

Version	Comment
1.1pre	First preliminary release
1.2	• Ethernet PHY requirements revised (e.g., link loss reaction time) • Added Microchip KSZ8001L • Added Texas Instruments DP83848, DP83849, and DP83640 • Editorial changes
1.3	• Added restriction to enhanced link configuration: RX_ER has to be asserted outside of frames (IEEE802 optional feature) • Removed Texas Instruments DP83848 and DP83849 temporarily for further examination
1.4	• Updated/clarified PHY requirements, PHY link loss reaction time is mandatory • Added Texas Instruments DP83848, DP83849 with comments • Added PHYs which require Enhanced Link detection to be activated • Editorial changes
1.5	• PHY startup should not rely on MDC clocking • Added Microchip KSZ8041NL/TL Rev. A4 to list of example Ethernet PHYs for EtherCAT with Enhanced Link Detection requirement • ESD tolerance and baseline wander compensation recommendations added • Editorial changes
1.6	• Completely revised and enhanced compatibility table • Editorial changes
1.7	• Added restrictions for ET1100-0002/ET1200-0002 and PHYs which require Enhanced Link Detection: PHY address offset must be 0 • PHY address offset for Teridian PHYs and Microchip KSZ8041 corrected
1.8	• Added Microchip KSZ8051 PHYs • Link loss reaction time of Broadcom BCM5241is higher than data sheet reports • Clarified suitability of some Microchip/Texas Instruments PHYs for ET1100, ET1200 • Changed footnote: Microchip PIC10 is expected to be not suitable for management address conversion during an access (PIC10 remains suitable for adding an extra MDC cycle)
2.0	• Microchip KSZ8051: update to rev. A2 • Microchip KSZ8721: LED1 speed behavior comments added • Texas Instruments DP83848/DP83849 comment on clock supply added • Renesas µPD60610, µPD60611, µPD60620, µPD60621 added • Microchip LAN8700 added • STMicroelectronics STE802RT1A/B PHYs added • Texas Instruments DP83620/ DP83630 added • Added chapter about EtherCAT over optical links • Added chapter about Gigabit Ethernet PHYs • Enhanced recommendations for Ethernet PHYs • Added recommendations to FX transceivers used for EtherCAT
2.1	• Added Texas Instruments TLK105, TLK106, and TLK110 • Added Microchip KSZ8081MNX,KSZ8081 MLX • Removed Microchip KSZ8721: not recommended for new designs by Microchip (Microchip recommends KSZ8051 or KSZ8081 instead) • Renesas µPD60610, µPD60611, µPD60620, µPD60621 updated • Added IC Plus Corp. IP101G • IEEE802.3az Energy Efficient Ethernet must not be used • Added required PHY signals table • Updated to ET1100-0003/ET1200 -0003
2.2	• Update to EtherCAT IP Core V3.0.2/V3.00c with FX support • RX_ER is required for EtherCAT • Editorial changes

Version	Comment
2.3	• Renesas µPD60610/µPD60611: Auto-TX-Shift required (data sheet was updated) • Renesas µPD60610/µPD60611/ µPD60620/µPD60621: MI link detection and configuration can only be enabled with certain IP Core versions • Texas Instruments TLK105/TLK106/TLK110: MI link detection and configuration must not be enabled • Microchip PHYs: added notes for an internal pull-up resistor at MDC pin • Added note for PHYs with Enhanced link detection recommendation • Editorial changes
2.4	• Microchip PHYs: added comments regarding SPEED LED usage • Added Microchip KSZ8061 • Added Texas Instruments TLK111 • PHY address offset recommendations for IP core relaxed because IP core supports any PHY address offset now.
2.5	• Added note regarding odd nibble detection for Texas Instruments TLK105, TLK106, TLK110, TLK111 • Updated requirements for Texas Instruments DP83xxx PHYs, especially DP83849 restrictions with ET1100/ET1200 • Added Texas Instruments DP83822 • Changed recommended PHY address offset for Texas Instruments DP83620/DP83630/DP83640/DP83848: use offset 16 with ET1100-0003/ET1200-0003
2.6	• Changed recommended PHY address offset for Microchip KSZ8001L: use offset 16 with ET1100-0003/ET1200-0003 • Added Davicom Semiconductor DM9162 and DM9163 • Added Microchip KSZ8091MLX • Added Microsemi VSC8530 and VSC8540 • Updated comments for Texas Instruments PHYs • Editorial changes
2.7	• Removed Marvell 88E3016 from incompatible PHY list, because IP Core supports RGMII • Added Analog Devices ADIN1200 • Added EtherCAT G chapter and devices Analog Devices ADIN1300, Broadcom B50212E, Marvell 88E1111 • Editorial changes
3.0	• Add reference to EtherCAT P • Remove ESC10/ESC20 • Clarify EtherCAT PHY requirements, add maintaining additional nibble • Broadcom B50212E: Disable EEE by µC/Management Interface • Broadcom BCM54210, BCM54210S, BCM54210SE, BCM54210E, BCM54210PE, BCM54214E, BCM54216E, BCM54220, BCM54220S, BCM54210, BCM54210S, BCM54210SE, BCM54210E, BCM54210PE, BCM54214E, BCM54216E, BCM54220, BCM54220S added • IC Plus IP101GA: Disable EEE by µC/Management Interface; update to GA device • IC Plus IP1001C added • Marvell 88E1111, 88E1510, 88E1510P, 88E1510Q, 88E1512, 88E1512P, 88E1518 added • MaxLinear MxL86110, MxL86111 added • Microchip VSC8530, VSC8540: update comments according to latest data sheet • Microchip LAN8720A, LAN8740A, LAN8741A, LAN88730, KSZ9031RNX, KSZ9131RNX, LAN8820, LAN8830, LAN8831, LAN8840, LAN8841 added • Realtek RTL8201FR/FRI, RTL8201FI, RTL8211F, RTL8211FS added • Texas Instruments PHYs: update comments • Texas Instruments DP83825, DP83826, DP83867CR, DP83867IRRGZ, DP83867IR, DP83867CS, DP83867IS, DP83867E, DP83869HM added • Editorial changes

CONTENTS

1 Overview

An EtherCAT Slave Controller (ESC) takes care of the EtherCAT communication as an interface between the EtherCAT fieldbus (Ethernet) and the slave application.

EtherCAT uses 100Mbit/s full duplex Ethernet communication. EtherCAT G uses 1,000Mbit/s full duplex Ethernet communication, and it also supports 100Mbit/s EtherCAT communication. EtherCAT Slave Controllers process Ethernet frames on the fly.

This application note provides an overview of the requirements to Ethernet PHYs used for EtherCAT and EtherCAT G devices. An example list of Ethernet PHYs currently expected to be suitable for EtherCAT/EtherCAT G is also provided.

This application note applies to the following Beckhoff EtherCAT Slave Controllers:

- ET1200-0003
- ET1100-0003
- EtherCAT IP Core for Altera®/AMD®(Xilinx®) FPGAs V3.0.2/V3.00c and later

Refer to the ESC data sheets for further information. The ESC data sheets are available from the Beckhoff homepage (http://www.beckhoff.com).

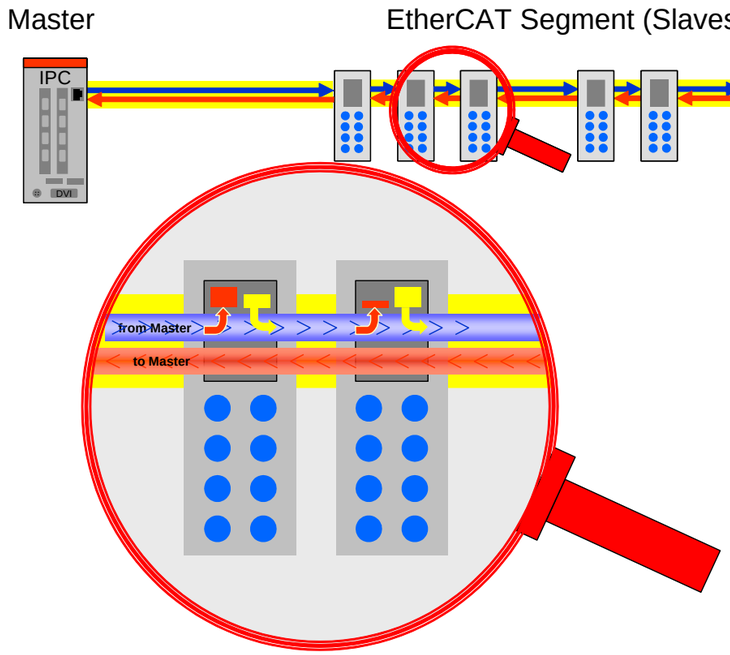

Figure 1: EtherCAT Segment

1.1 EtherCAT P

For EtherCAT P, with integrated power supply, there are further requirements, described in the *EtherCAT P Implementation Guide*, available at the EtherCAT Technology Group homepage (http://www.ethercat.org).

2 EtherCAT (100Mbit/s)

This chapter is about Ethernet PHYs used for Beckhoff ESCs which support EtherCAT only (not EtherCAT G). For EtherCAT, the **recommended interface is MII**, since RMII/RGMII PHYs include TX FIFOs which increase the forwarding delay of an EtherCAT slave device, as well as the forwarding jitter.

EtherCAT and Beckhoff ESCs have some general requirements to Ethernet PHYs, which are typically fulfilled by state-of-the-art Ethernet PHYs. Refer to Section III of the ESC documentation for ESC specific information and supported features.

2.1 Requirements

2.1.1 General requirements

The PHYs have to comply with **IEEE 802.3 100BaseTX or 100BaseFX**, including:

- The PHYs have to support 100 Mbit/s Full Duplex links.
- The PHYs have to provide an **MII** (or RMII/RGMII[1]) interface.
- The PHYs have to use autonegotiation in 100BaseTX mode.
- The PHYs have to support the MII management interface.
- The PHYs have to support MDI/MDI-X auto-crossover in 100BaseTX mode.
- The PHYs must **not modify the preamble** length.
- The PHYs must **not use IEEE802.3az Energy Efficient Ethernet**.
- Minimum cable length is 0 m
- The PHYs must offer the RX_ER signal (MII/RMII), or RX_ER as part of the RX_CTL signal (RGMII). RX_ER must indicate invalid symbols both during frames and during inter-frame gap.
- The PHYs must maintain an **additional nibble** at the end of a frame (odd nibble, dribble nibble), without marking it with an RX_ER.
- The PHYs have to provide a **signal indicating a 100 Mbit/s (Full Duplex) link**[2], typically a configurable LED output. The signal polarity is active low or configurable for some ESCs. For RGMII, in-band status is sufficient, which should be enabled by default.

2.1.2 Additional requirements using Beckhoff ESCs

PHY address
The Beckhoff ESCs use a shared MII Management Interface, so up to 4 different PHY addresses are required. The **PHY addresses 0-3 are recommended**, no address should be used as broadcast/isolate address.

When the PHY does not support addresses 0-3, the specific ESC features must be checked:

- Most ESCs require consecutive PHY addresses, except for the EtherCAT IP Core, which requires up to 3 individual addresses.
- Some ESCs also support a fixed offset, e.g. offset 16 for PHY addresses 16-19, or offset 1 for PHY addresses 1-4. Recommendation is to use offset 16, if that is not possible, offset 1.

PHY configuration
There is not necessarily a µController available in an EtherCAT device, which can configure a PHY. Therefore, PHY configuration must not rely on configuration via the MII management interface, i.e., required features must be enabled after power-on[3], e.g., by default or by **strapping options**.

Only the EtherCAT IP Core supports basic configuration via MII management interface, especially advertisement of 100 Mbit/s Full Duplex when using Gigabit PHYs (MI Link detection and configuration). Any further configuration requires a µController attached to the ESC.

[1] RMII/RGMII is only supported by the EtherCAT IP Core
[2] If a combined signal (100 MBit/s link with Full Duplex) is not available, a signal indicating a 100 Mbit/s link might be used. Take care that the link signal is inactive in case of no link. If only a Link signal is available, this might be used. Never use (combined) activity signals. Some PHYs toggle the 100 Mbit/s speed signal during autonegotiation, this is a problem for hot-connecting. Use a link signal in this case.
[3] This is especially true for: link LED enable, EEE disable, preamble/additional nibble maintenance, RGMII in-band status enable.

MDC
MII Management interface should not require additional MDC cycles, nor continuous MDC. PHY startup should not rely on MII management interaction, i.e., MDC clocking, since many ESCs do not communicate with the PHY via management interface unless the EtherCAT master requests this.

2.1.3 Additional requirements using Beckhoff ESCs with MII Interface

The MII interfaces of Beckhoff ESCs are optimized for low processing/forwarding delays by **omitting a transmit FIFO**. To allow this, the Beckhoff ESCs have additional requirements to Ethernet PHYs, which are easily accomplished by several PHY vendors

All PHYs connected to one ESC and the ESC itself must share the **same clock source**, so a TX FIFO can be omitted. This can be achieved by sourcing the PHYs from an ESC clock output or by sourcing the PHYs and the ESC from the same quartz oscillator. The phase offset between TX_CLK and the clock input of the PHYs is compensated inside the ESC, either manually by configuration or automatically. The clock period cannot change between the PHYs and the ESC, since they have to share the same clock source.

There are two options for adjusting the phase relation of TX_EN/TXD (generated by ESC) in relation to TX_CLK (generated by the PHY):

- **Manual TX Shift compensation**:
  A static signal delay for TX_EN/TXD by 0/10/20/30 ns is configured, which is used for all MII ports. Thus, **all PHYs** connected to one ESC must have the **same fixed phase relation** between TX_CLK and the clock input of the PHY. The phase relation must be the same each time the PHYs are powered up/establish a link. The TX_CLK signal is not connected to the ESC.
- **Automatic TX Shift compensation** (IP Core only):
  The ESC detects the required phase shift automatically, based on the TX_CLK signal. This is not the same function as a TX FIFO, the clock source still must be the same. But the PHYs are not required to have the same fixed phase relation each time they are powered on/establish a link.

2.2 Recommendations

2.2.1 General recommendations

- Receive and transmit delays should be deterministic, and as low as possible. They should comply with the standard (RX delay should be below ~320 ns, TX delay below ~140 ns).
- PHY link loss reaction time (link loss to link signal/LED output change) should be faster than 15 µs to enable redundancy operation. Otherwise, Enhanced link detection in the ESC must be enabled. Enhanced link detection uses the RX_ER signal, and it requires that the PHY asserts RX_ER both inside and outside of frames for each invalid symbol. Enhanced link detection requires proper PHY address configuration.
- The PHYs should detect link loss within the link loss reaction time of 15 µs also if only one of the RX+ and RX- lines gets disconnected.
- ESD tolerance should be as high as possible (4kV or better)
- MDC should not incorporate pull-up/pull-down resistors, as this signal is used as a configuration input signal by some ESCs.
- PHY addresses should identify individual PHYs, using address 0-3. A broadcast address, or default isolate address can cause issues with supported PHY addresses.
- Power consumption should be as low as possible.
- I/O voltage: 3.3V should be supported for current ASIC and FPGA ESCs, additional 2.5V/1.8V I/O support is recommended for recent FPGA ESCs.
- Single power supply according to I/O voltage.
- The PHY should use a 25 MHz clock source (quartz oscillator or ESC output).
- Industrial temperature range should be supported.

2.2.2 Recommendations for 100BaseTX

- Maximum cable length should be ≥ 120 m to maintain a safety margin if the standard maximum cable length of 100 m is used.
- Baseline wander should be compensated (the PHYs should cope with the ANSI X3.263 DDJ test pattern for baseline wander measurements at maximum cable length, without frame loss).
- Restriction of Autonegotiation advertisement to 100 Mbit/s / Full Duplex is desirable (configured by hardware strapping options).

2.2.3 Recommendations for 100BaseFX

- Ethernet PHYs for 100BaseFX should implement Far-End-Fault (FEF) completely (generation and detection).
- The transceiver should have an input for disabling the transceiver/transmitter (for Enhanced FX link detection; e.g. enable, power-down or reset).

2.3 Example PHYs

In this chapter, some example Ethernet PHYs which are assumed to fulfill the EtherCAT requirements are presented, as well as an overview of Ethernet PHYs which are assumed to not fulfill these requirements. These lists represent a current collection of information from data sheets, vendors, and basic hardware tests for some devices, and they represent the best of **current knowledge**. These lists do not imply any kind of certification for EtherCAT, since none of these PHYs has been tested thoroughly to fulfill each individual EtherCAT or IEEE802.3 requirement. These lists are only intended for sharing current information about Ethernet PHYs for EtherCAT, and they are still **work-in-progress**.

The Ethernet PHYs were either judged by a **brief** overview of their data sheets or by additional **basic** hardware communication tests (basic hardware communication tests are indicated in the table).

The example Ethernet PHYs for EtherCAT shown in the following tables are sorted alphabetically by vendor name, not by preference. The selection of Ethernet PHYs was restricted to 1-4 port 10/100 Mbit/s Ethernet PHYs. These tables are incomplete in terms of Ethernet PHY vendors and Ethernet PHY devices – they just give some examples, and it is likely that other devices and devices from many vendors meet the requirements as well.

It cannot be guaranteed that the mentioned Ethernet PHYs, future revisions of them, or product changes are or will be fully EtherCAT compatible or not, nor that they are compatible with individual ESCs – because of ESC specific options (e.g., configurable link polarity, supported PHY address offsets, Enhanced Link detection, automatic TX Shift compensation). As far as known, restrictions and features of the PHYs impacting their EtherCAT usage are added to the tables.

Table 1 indicates for which ESC the PHY is assumed to be suitable, and which features have to be enabled and which settings have to be made for the ESC/PHY combination.

The main criteria are:

TX_CLK fixed phase, Auto TX Shift
Some Ethernet PHYs cannot guarantee a fixed phase relation between their clock input and TX_CLK. The Auto TX Shift feature compensates these phase shift variations. Auto TX Shift is not equivalent to a TX FIFO, it is just a controlled output phase for the TX signals. ESC and PHY have to share the same clock source anyway.

PHYs without a fixed phase for TX_CLK require Auto TX Shift to be activated.

PHY address, PHY address offset
All ESCs support PHY addresses 0-3 for ports 0-3. ET1200/ET1100 also support an offset of 16, using PHY address 16-19. Future ESCs can support an offset of 1, using PHY address 1-4. The IP core since version 3.0.0 supports independent PHY addresses (including non-consecutive addresses).

Link signal
A link signal is required for MII/RMII. The ET1200 requires an active low signal, while ET1100 and IP core are configurable. For RGMII, In-band status is required.

Link loss reaction time, Enhanced Link Detection
Some Ethernet PHYs require **Enhanced Link Detection** to be activated in order to achieve sufficient link loss reaction times. Enhanced Link Detection is generally recommended because additional faults are detected and link loss reaction time is improved. Additionally, using Enhanced Link Detection allows an application specific configuration (robust communication vs. redundancy operation).

For back-to-back connections, Enhanced Link Detection must not be activated.

EEE (Energy Efficient Ethernet)
EtherCAT cannot use EEE, thus advertisement and usage have to be disabled. It must be disabled by default, by strapping, or using an additional µController, which disables this feature in the PHY using the PHY management interface.

2.3.1 Example PHYs compatible with EtherCAT

Table 1: Example Ethernet PHYs assumed to fulfill EtherCAT requirements

Vendor / Device	# Ports	ET1200 suitable	ET1100 suitable	IP Core suitable	Basic HW test[4]	TX_CLK fixed phase[5]	Auto-TX-Shift (IP Core only)	PHY addr.[6]	PHY addr. offset[7]	Link loss reaction time	Enhanced Link Detection	Comments
Analog Devices												
78Q2123 78Q2133	1			X			provisionally	0/1	0		provisionally	PHY addr. 0 = Broadcast. Only for single port devices, because only one PHY address can be used.
ADIN1200	1	-	X	X	yes	yes (Data sheet)		0-15	0	0.6 µs	recommended[9]	
Broadcom												
BCM5221	1	X	X	X		yes (Data sheet[8])		0-31	0	1.3 µs	recommended[9]	Requires additional write clock on MDC (supported by ET1100-0003, ET1200-0003, IP Core since v2.3.1/2.03b). Quartz oscillator required. Internal pull-down at MDC.
BCM5222	2	X	X	X		yes (Data sheet)		0-31	0	1.3 µs	recommended[9]	Requires additional write clock on MDC (supported by ET1100-0003, ET1200-0003, IP Core since v2.3.1/2.03b). Quartz oscillator required. Internal pull-down at MDC.
BCM5241	1	X	X	X	yes	yes (Data sheet)		0-7, 8, 16, 24	0	45 µs	required	Requires additional write clock on MDC (supported by ET1100-0003, ET1200-0003, IP Core since v2.3.1/2.03b). Quartz oscillator required. Internal pull-up at MDC. XTALI voltage ≤ 1.8V.
Davicom Semiconductor												
DM9161B	1			X			provisionally	0-31	0		provisionally	
DM9162	1	-	-	X		no	required	0-31	0	1.79ms	required	
DM9163	1	-	-	X		no	required	0-31	0	1.79ms	required	
IC Plus Corp.												
IP101ALF	1			X			provisionally	0-31	0		provisionally	Link signal polarity depends on PHY address.
IP101GA	1			X			provisionally	0-7	0		provisionally	Link signal polarity depends on PHY address. Disable EEE by µC/Management Interface.
Marvell												
88E3015 88E3018	1	-	-	X		no	required	0-31	0		provisionally	
LXT973	2	(X)	(X)	X	yes	probably	provisionally	0-31	0	1.9 ms	required	Measurements from the vendor with some LXT973 indicated that there is a fixed TX_CLK phase relation, but a general statement could not be made. It is assumed that Auto-TX-Shift is not required and that ET1200/ET1100 are supported.

[4] The following requirements were not part of the basic hardware test: MDI/MDI-X auto-crossover, MII management interface, TX clock phase relation, and preamble length maintenance. These requirements are assumed to be fulfilled either according to the data sheet or vendor notice. Hardware tests are typically performed with only one of the ESC types, e.g., IP Core.
[5] Information about fixed phase shift between TX_CLK and PHY clock source from data sheet or from vendor
[6] PHY address range supported by PHY. Special PHY addresses are excluded (Broadcast/Isolate/Power down).
[7] Suggested PHY address offset. ET1100 and ET1200 only support a PHY address offset of 0 or 16. A PHY address offset of 0 means PHY addresses 0-3 are used, an offset of 16 means PHY addresses 16-19 are used, etc..
[8] Only for XTALI, not approved for REF_CLK. According to Broadcom, a quartz oscillator can be connected to XTALI as well.
[9] Recommended for IP Core only. Should not be enabled for ET1100/ET1200 (otherwise there is a potential risk of an additional link-down/link-up-cycle caused by ET1100/ET1200 directly after the link is re-established.

Vendor / Device	# Ports	ET1200 suitable	ET1100 suitable	IP Core suitable	Basic HW test[4]	TX_CLK fixed phase[5]	Auto-TX-Shift (IP Core only)	PHY addr.[6]	PHY addr. offset[7]	Link loss reaction time	Enhanced Link Detection	Comments
Microchip												
KSZ8001L KSZ80010S	1	X	X	X		yes (Vendor)		1-31	16		provisionally	PHY addr. 0 = Broadcast. The KSZ8001 might have a pull-up resistor at the MDC pin, which might interfere with an external pull-down resistor for strapping. The SPEED LED might toggle during link up, causing lost frames for a short period. Either enable MI Link Detection and Configuration or use LINK LED (requires enabling via management interface).
KSZ8041TL KSZ8041NL KSZ8040FTL	1	-	-	X		yes (Vendor)		1-7	1	10 µs	recommended[9]	Minimum Revision A4, which supports preamble maintenance. PHY addr. 0 = Broadcast. Enable 8 byte preamble with CONFIG[2:0]=100 (was PCS Loopback in Rev. A3). The SPEED LED might toggle during link up, causing lost frames for a short period. Either enable MI Link Detection and Configuration or use LINK LED (requires enabling via management interface). The KSZ8041 might have a pull-up resistor at the MDC pin, which might interfere with an external pull-down resistor for strapping.
KSZ8051 MLL KSZ8051 MNL	1	X	X	X		yes (Vendor)		0-7	0	5.3 µs	recommended[9]	Minimum revision A2, which has a fixed TX_CLK phase. Enable B_CAST_OFF to support PHY addr. 0 (otherwise PHY addr. 0 = Broadcast). The KSZ8051 might have a pull-up resistor at the MDC pin, which might interfere with an external pull-down resistor for strapping. The SPEED LED might toggle during link up, causing lost frames for a short period. Either enable MI Link Detection and Configuration or use LINK LED (requires enabling via management interface).
KSZ8061MNX	1	-	-	X		yes (Data sheet)		1-7	1	4.8 µs	recommended	Disable Fixed RX PHY latency via management interface, otherwise preamble reduction possible. PHY addr. 0 = Broadcast.
KSZ8061MNG	1	X[10]	X[10]	X		yes (Data sheet)		0-7	0	4.8 µs	recommended[9]	Disable Fixed RX PHY latency via management interface, otherwise preamble reduction possible. Enable B_CAST_OFF to support PHY addr. 0 (otherwise PHY addr. 0 = Broadcast). The SPEED LED might toggle during link up, causing lost frames for a short period. Either enable MI Link Detection and Configuration or use LINK LED (requires enabling via management interface).
KSZ8061RNB KSZ8061RND	1	-	-	X		n. a.		1-7	1	4.8 µs	recommended	RMII only. Disable Fixed RX PHY latency via management interface, otherwise preamble reduction possible. PHY addr. 0 = Broadcast. The SPEED LED might toggle during link up, causing lost frames for a short period. Either enable MI Link Detection and Configuration or use LINK LED (requires enabling via management interface).
KSZ8081MNX KSZ8081MLX	1	X	X	X		yes (Data sheet)		0-7	0	4.4 µs	recommended[9]	Enable B_CAST_OFF to support PHY addr. 0 (otherwise PHY addr. 0 = Broadcast). The KSZ8081 has a pull-up resistor at the MDC pin, which might interfere with an external pull-down resistor for strapping. The SPEED LED might toggle during link up, causing lost frames for a short period. Either enable MI Link Detection and Configuration or use LINK LED (requires enabling via management interface).
KSZ8091MLX	1	X	X	X		yes (Data sheet)		0-7	0	4.4 µs	recommended[9]	Enable B_CAST_OFF to support PHY addr. 0 (otherwise PHY addr. 0 = Broadcast). The KSZ8091 has a pull-up resistor at the MDC pin, which might interfere with an external pull-down resistor for strapping. The SPEED LED might toggle during link up, causing lost frames for a short period. Either enable MI Link Detection and Configuration or use LINK LED (requires enabling via management interface).
LAN8187	1	-	-	X		no (Vendor)	required	0-31	0		provisionally	Link signal polarity depends on PHY address.
LAN8700	1	-	-	X		no (Vendor)	required	0-31	0		provisionally	Link signal polarity depends on PHY address.
LAN8710A	1	-	-	X		no	required	0-7	0		provisionally	
LAN8720A	1	-	-	X		n. a.		0-1	0		provisionally	RMII only.
LAN8740A	1	-	-	X			provisionally	0-7	0		provisionally	
LAN8741A	1	-	-	X			provisionally	0-7	0		provisionally	
LAN88730	1	-	-	X			provisionally	0-7	0		provisionally	
VSC8530	1	-	-	X		no (Vendor)	required	0 or 0-31	0	10 µs	not necessary	RMII/RGMII only. LED configuration to Fast Link Fail by µC/management interface required. Unmanaged mode: EEE disable by µC/management interface required, only PHY address 0 Managed mode: MAC interface configuration by µC/management interface required
VSC8540	1	-	-	X		no (Vendor)	required	0-3 or 0-31	0	10 µs	not necessary	LED configuration to Fast Link Fail by µC/management interface required. Unmanaged mode: EEE disable by µC/management interface required. Managed mode: MAC interface configuration by µC/management interface required

[10] ET1100/ET1200 do not support/fully support MI management access from the µController, so external logic is required to access the PHY.

Vendor / Device	# Ports	ET1200 suitable	ET1100 suitable	IP Core suitable	Basic HW test[4]	TX_CLK fixed phase[5]	Auto-TX-Shift (IP Core only)	PHY addr.[6]	PHY addr. offset[7]	Link loss reaction time	Enhanced Link Detection	Comments
Realtek												
RTL8201N	1	-	-	X		no (Vendor)	required	1-31	16		provisionally	PHY addr. 0 = Power down.
RTL8201DL	1	-	-	X		no (Vendor)	required	0-7	0		provisionally	
RTL8201FR RTL8201FRI	1	-	-	X		n. a.		0-1	0		provisionally	RMII only. Configure link LED (LED1=LINK100) and disable EEE by µC/Management Interface
RTL8201FI	1	-	-	X			provisionally	0-3	0		provisionally	Configure link LED (LED1=LINK100) and disable EEE by µC/Management Interface
Renesas												
µPD60610 µPD60611	1	-	-	X		no	required	0/8/16/24	0	3 x RX_ER (120 ns)	not necessary	MI Link detection and configuration can only be enabled for IP Cores starting with V2.4.3/V2.04d and V3.0.2/V3.00c Link loss reaction time configurable via MII management interface.
µPD60620A µPD60621A	2	X	X	X		yes (Data sheet)		0/8/16/24+1	0	3 x RX_ER (120 ns)	not necessary	Set P1TXCL=0 for fixed TX_CLK phase shift. EtherCAT support starts with order number UPD60620AGK-GAK-AX / UPD60621AGK-GAK-AX. MI Link detection and configuration can only be enabled for IP Cores starting with V2.4.3/V2.04d and V3.0.2/V3.00c Link loss reaction time configurable via MII management interface.
STMicroelectronics												
STE101P	1	-	-	X			provisionally	1-31	16		provisionally	PHY addr. 0 = Isolate. MDC clock transition required to complete reset phase (MI Link Detection and Configuration required). Link signal polarity depends on PHY address.
STE802RT1A STE802RT1B	1	-	-	X		yes (Vendor)		1-31	16		provisionally	PHY addr. 0 = Isolate. MDC clock transition required to complete reset phase (MI Link Detection and Configuration required).

Vendor / Device	# Ports	ET1200 suitable	ET1100 suitable	IP Core suitable	Basic HW test[4]	TX_CLK fixed phase[5]	Auto-TX-Shift (IP Core only)	PHY addr.[6]	PHY addr. offset[7]	Link loss reaction time	Enhanced Link Detection	Comments
Texas Instruments												
DP83620 DP83630 DP83640	1	X	X	X		yes (Vendor)		1-31	16	250 µs (conf. to ~1.3 µs)	required	PHY addr. 0 = Isolate. Do not use SCMII mode. Use LED_LINK for link detection. X1 must not be floating, add 2.2KΩ pull-down if necessary (e.g., ET1100/ET1200: CLK25Out is not driven before strapping).
DP83822	1	X	X	X		yes (Data sheet)		0-31	0	250 µs (conf. to <10 µs)	required	Disable Odd nibble detection via MII management, otherwise Forwarded RX errors cannot be detected. Use LED_LINK for link detection. X1 must not be floating, add 2.2KΩ pull-down if necessary (e.g., ET1100/ET1200: CLK25Out is not driven before strapping). Fast Link Down mode with 10 µs reaction time is supported. Recommended configuration for Fast Link Down mode in CR3: enable Bit 10 (Descrambler), Bit 3 (RX Error count) and Bit 2 (MLT3 error). RGMII mode: TX_CLK is driven up to 200ns after reset release.
DP83825	1	-	-	X		n. a.		0-3	0	200 µs (conf. to <5 µs)	required	RMII only. MI Link detection and configuration must not be used for IP Cores, because register 9 is PHY specific.
DP83826	1	(X)	X	X		yes (Data sheet)		0-7	0	Basic: 200 µs (conf. to <5 µs) Enhanced: <5 µs	Basic mode: provisionally	Rev. B and later only. MI Link detection and configuration must not be used for IP Cores, because register 9 is PHY specific. Basic mode: - Link signal polarity configurable (act. low, LED1) - Disable Odd nibble detection via MII management, otherwise Forwarded RX errors cannot be detected - Fast Link Down mode with 5 µs reaction time is configured via MII management. Recommended configuration for Fast Link Down mode in CR3: enable Bit 10 (Descrambler), Bit 3 (RX Error count) and Bit 2 (MLT3 error), and FLD_CFG2: Bit [5:0] = 0x08 Enhanced mode: - Disable Odd nibble detection via strap1, otherwise Forwarded RX errors cannot be detected - Fast Link Down mode with 5 µs reaction time is configured via strapping and MII management. Recommended configuration for Fast Link Down mode in CR3: enable Bit 10 (Descrambler), Bit 3 (RX Error count) and Bit 2 (MLT3 error), and FLD_CFG2: Bit [5:0] = 0x08
DP83848	1	X	X	X	yes	yes (Vendor)		1-31	16	250 µs	required	PHY addr. 0 = Isolate. Use LED_LINK for link detection. X1 must not be floating, add 2.2KΩ pull-down if necessary (e.g., ET1100/ET1200: CLK25Out is not driven before strapping).
DP83849	2	X	X	X		yes (Vendor)		0-31	0	250 µs	required	Do not use SCMII mode. Use LED_LINK for link detection. X1 must not be floating, add 2.2KΩ pull-down if necessary. TXD is potentially driven by PHY before a clock signal is applied to X1 (ET1100/ET1200: CLK25Out cannot be used, an external clock source is required).
TLK100	1	-	-	X		no	required	0-31	0	500 µs	required	TX_CLK phase changes at each link up.
TLK105	1	X	X	X		yes (Data sheet)		0-31	0	200 µs (conf. to <10 µs)	required	Disable Odd nibble detection via MII management, otherwise Forwarded RX errors cannot be detected. Fast Link Down mode with 10 µs reaction time is supported (requires configuration via MII management, default is 200 µs). Recommended configuration for Fast Link Down mode in CR3: enable Bit 3 (RX Error count) and Bit 2 (MLT3 error). MI Link detection and configuration must not be used for IP Cores, because register 9 is PHY specific.
TLK106	1	X	X	X		yes (Data sheet)		0-31	0	200 µs (conf. to <10 µs)	required	Disable Odd nibble detection via MII management, otherwise Forwarded RX errors cannot be detected. Fast Link Down mode with 10 µs reaction time is supported (requires configuration via MII management, default is 200 µs). Recommended configuration for Fast Link Down mode in CR3: enable Bit 3 (RX Error count) and Bit 2 (MLT3 error). MI Link detection and configuration must not be used for IP Cores, because register 9 is PHY specific.
TLK110	1	X	X	X		yes (Data sheet)		0-31	0	200 µs (conf. to <10 µs)	required	Disable Odd nibble detection via MII management, otherwise Forwarded RX errors cannot be detected. Fast Link Down mode with 10 µs reaction time is supported (requires configuration via MII management, default is 200 µs). Recommended configuration for Fast Link Down mode in SWSCR3: enable Bit 3 (RX Error count) and Bit 2 (MLT3 error). MI Link detection and configuration must not be used for IP Cores, because register 9 is PHY specific.
TLK111	1	X	X	X		yes (Data sheet)		0-31	0	200 µs (conf. to <10 µs)	required	Disable Odd nibble detection via MII management, otherwise Forwarded RX errors cannot be detected. Fast Link Down mode with 10 µs reaction time is supported (requires configuration via MII management, default is 200 µs). Recommended configuration for Fast Link Down mode in SWSCR3: enable Bit 3 (RX Error count) and Bit 2 (MLT3 error). MI Link detection and configuration must not be used for IP Cores, because register 9 is PHY specific.

2.3.2 Example PHYs incompatible with EtherCAT

The following Ethernet PHYs are currently assumed or known to be **incompatible** with EtherCAT – because they do not support MDI/MDIX-auto-crossover which became state-of-the-art for many recent PHYs:

- AMD: Am79C874, Am79C875 (datasheet: no MDI/MDIX-auto-crossover)
- Analog Devices: 78Q2120C (datasheet: no MDI/MDIX-auto-crossover)
- Broadcom: BCM5208R (datasheet: no MDI/MDIX-auto-crossover)
  BCM5214 (datasheet: only RMII/SMII interface)
- Davicom Semiconductor: DM9161 (datasheet: no MDI/MDIX-auto-crossover)
- Marvell: LXT970A, LXT971A, LXT972A, LXT972M, LXT974, LXT975 (datasheet: no MDI/MDIX-auto-crossover)
- Microchip: KSZ8041 Rev. A3 (hardware test: no preamble maintenance) and maybe previous revisions
  LAN83C185 (datasheet: no MDI/MDIX-auto-crossover)
- STMicroelectronics: STE100P (datasheet: no MDI/MDIX-auto-crossover)
- VIA Technology: VT6103F, VT6303L (datasheet: no MDI/MDIX-auto-crossover)

2.4 PHY connection

Figure 2 shows the principle connection between ESC[11] and PHY. The clock source of Ethernet PHYs and ESC has to be the same quartz or quartz oscillator. TX_CLK is usually not connected unless automatic TX Shift compensation is used, because the ESCs do not incorporate a TX FIFO. The TX signals can be delayed inside the ESC for TX_CLK phase shift compensation. LINK_STATUS is an LED output indicating a 100 Mbit/s (Full Duplex) link.

Refer to ESC data sheet Section III for details about Ethernet PHY connection of a specific ESC.

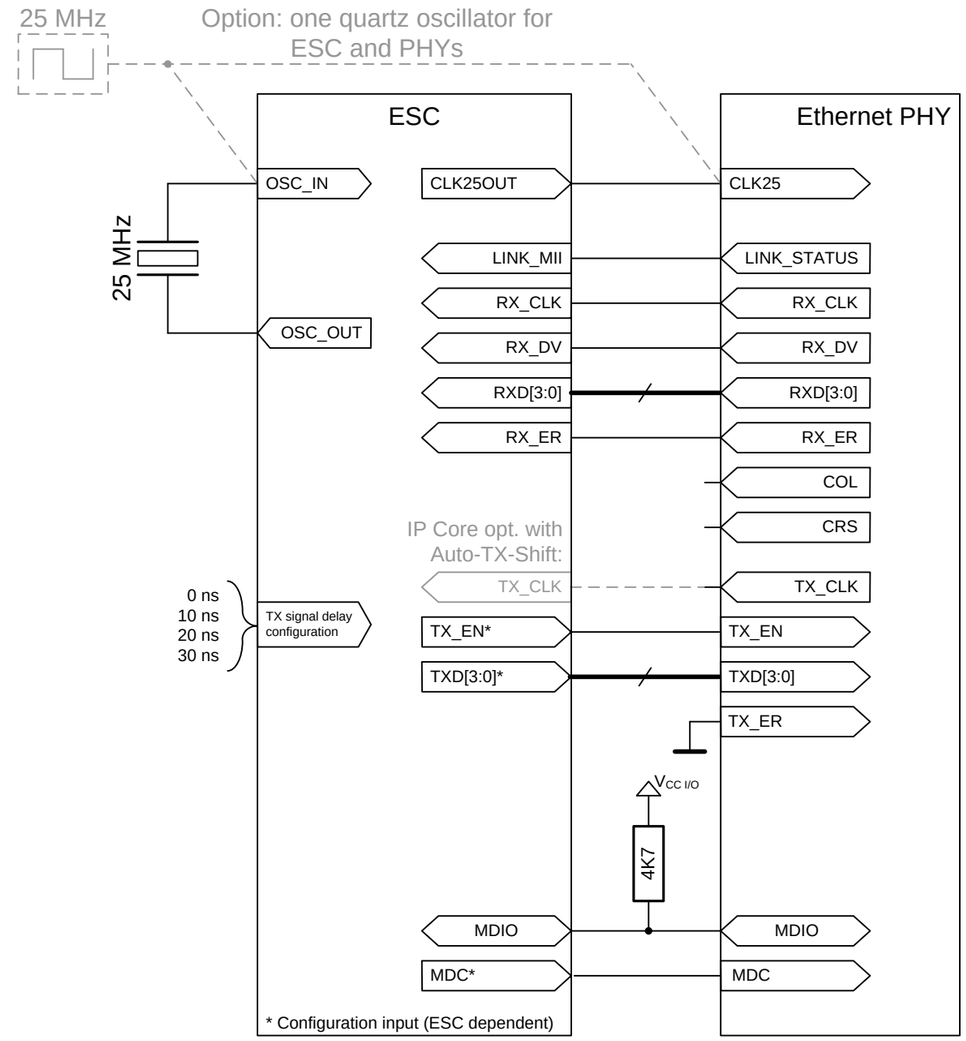

Figure 2: PHY Connection (MII)

[11] FPGAs with IP Core only support the quartz oscillator alternative.

2.4.1.1 Required Ethernet PHY signals

Table 2: Required Ethernet PHY signals using MII

Signal	Required	Comment
CLK25	Mandatory	Shared 25 MHzclock source between ESC and PHY
LINK_STATUS	Mandatory	LINK LED signal, required for fast link loss reaction time
RX_CLK	Mandatory	
RX_DV	Mandatory	
RXD[3:0]	Mandatory	
RX_ER	Mandatory	Required for error detection and error source localization
COL	Not used	EtherCAT uses full duplex only
CRS	Not used	EtherCAT uses full duplex only
TX_CLK	Optional	Optional for automatic TX Shift compensation
TXD[3:0]	Mandatory	
TX_ER	Not used	Connect to GND
MDIO	Optional	Recommended especially for debugging
MDC	Optional	Recommended especially for debugging

Table 3: Required Ethernet PHY signals using RMII

Signal	Required	Comment
REF_CLK	Mandatory	Shared 50 MHz clock source between ESC and PHY
LINK_STATUS	Mandatory	LINK LED signal, required for fast link loss reaction time
CRS_DV	Mandatory	
RXD[1:0]	Mandatory	
RX_ER	Mandatory	Required for error detection and error source localization
TX_EN	Mandatory	
TXD[1:0]	Mandatory	
MDIO	Optional	Recommended especially for debugging
MDC	Optional	Recommended especially for debugging

Table 4: Required Ethernet PHY signals using RGMII

Signal	Required	Comment
RX_CLK	Mandatory	
RX_CTL	Mandatory	
RXD[3:0]	Mandatory	Mandatory: RGMII In-band status for fast link loss reaction time
TX_CLK	Mandatory	
TX_CTL	Mandatory	
TXD[3:0]	Mandatory	
MDIO	Optional	Recommended especially for configuration and debugging
MDC	Optional	Recommended especially for configuration and debugging

2.5 Clock supply

The initial accuracy at room temperature of the PHY clock source has to be 25 ppm or better. This enables FIFO size reduction, i.e., forwarding delay reduction, and supports fast DC locking.

2.6 Gigabit Ethernet PHYs used for EtherCAT (100Mbit/s)

Gigabit Ethernet PHYs can generally be used for EtherCAT, as long as the link speed is restricted to 100 Mbit/s, either by strapping options of the PHY, or by using the autonegotiation advertisement.

Some ESCs are capable of restricting the autonegotiation advertisement of Gigabit Ethernet PHYs to 100 Mbit/s full-duplex if MI link detection and configuration is enabled.

All PHYs suitable for EtherCAT G can also be used for EtherCAT, since EtherCAT G is compatible with EtherCAT. Nevertheless, due to the higher latency of Gigabit Ethernet PHYs, it is recommended to use 100 Mbit/s Ethernet PHYs.

The requirements to Ethernet PHYs for EtherCAT G apply, especially enhanced link detection needs to be enabled (unless the link loss reaction time of the PHY is below 15 µs).

2.7 EtherCAT over optical links (100Base-FX)

The intention of this chapter is to **share current knowledge** about FX operation with EtherCAT. The solutions and comments are still **work-in-progress**, they are possibly subject to change or even incomplete. Most of the presented example schematics have not been implemented in hardware, but they are expected to be working.

2.7.1 ESCs with native FX support

ESCs with FX support have individual PHY reset outputs for each port. This PHY reset output is intended to hold the PHY and the transceiver in reset state while the ESC is in reset state, and additionally, to issue a reset cycle when a link failure is detected by the enhanced link detection mechanism.

If at least one port is configured for FX operation, all ports have to use the individual PHY reset outputs. This is especially important for enhanced link detection, since all the PHY reset outputs are used for link down signalling instead of auto-negotiation restart, which is not used anymore – regardless of the port using FX or TX.

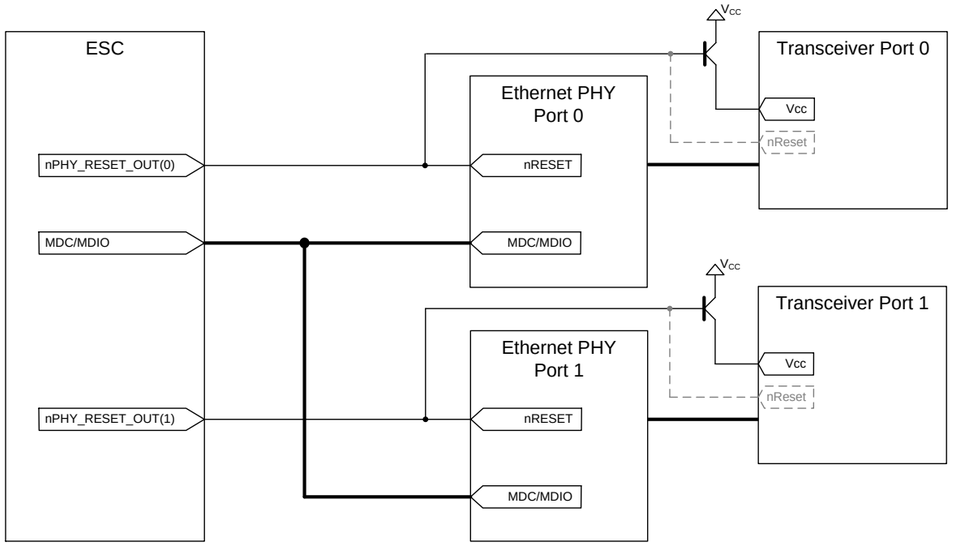

Figure 3: PHY reset connection for ESCs with FX support or mixed FX/TX support

2.7.2 ESCs without native FX support

2.7.2.1 Standard Link Detection

The Enhanced link detection restarts auto-negotiation between the PHYs if a certain level of receive errors is reached. With FX PHYs, auto-negotiation is not available (it is a 100Base-TX feature). Typically, PHYs ignore

the restart auto-negotiation request. As a consequence, the EtherCAT slave controller waits endlessly for the link to go down. Other PHYs might get into a dead-lock, because auto-negotiation is enabled by the restart auto-negotiation request, but it will not complete due to the FX operation mode.

Thus, Enhanced Link Detection has to be turned off for FX links (unless Enhanced FX Link Detection is used, which is recommended. See later for more information). It is strongly recommended to use PHYs which are supporting Far-end-Fault (FEF) completely if Enhanced link detection is not used (refer to Section I of the ESC data sheets for more information on FEF).

2.7.2.1.1 Issue: Temporary Enhanced Link Detection while EEPROM is loading

Enhanced Link Detection is enabled after Reset, and it can only be disabled by EEPROM. This takes about 170 ms. In the meantime, the FX PHYs are powering up. Since they do not need to go through an auto-negotiation sequence, the link (signal detect) comes very early. It is possible that the link is detected, but communication is not possible (RX_ERR are detected). This can trigger the ESC to restart auto-negotiation before the EEPROM is loaded, resulting in potential PHY problems with the restart auto-negotiation request.

The recommended solution to overcome this issue is to power up the FX PHY (and the transceiver) at least 170 ms after the ESC, e.g. by an additional reset controller with delay or power sequencing (Figure 4 or Figure 5).

Another, recommended solution is the Enhanced FX Link Detection, discussed later.

2.7.2.1.2 Minimum solutions with Standard Link Detection

These two solutions represent the minimum solution for proper power-up and reset operation, but they have drawbacks in detection low quality links. The preferred solution is the Enhanced FX Link Detection, see later.

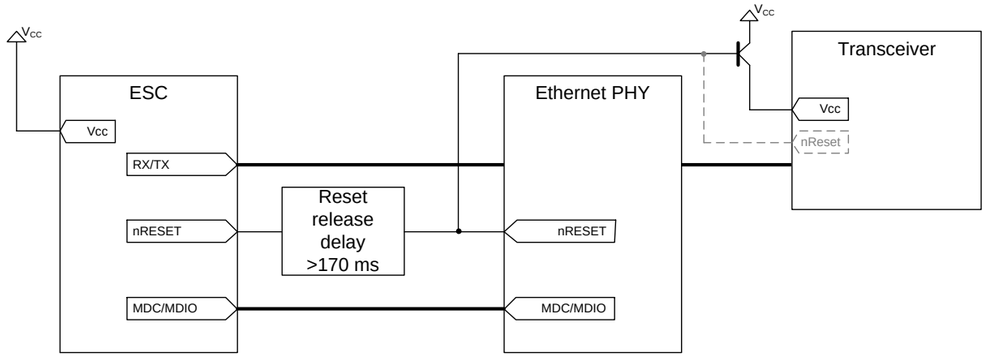

Figure 4: PHY reset release delay with transceiver power down/reset

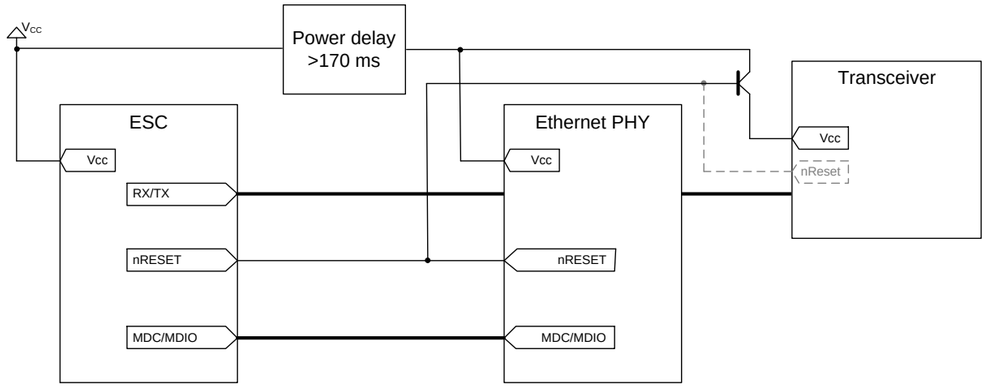

Figure 5: PHY power sequencing with transceiver power down/reset

2.7.2.2 Enhanced FX link detection

In order to detect erroneous links fast enough, it is desirable to use the error detection principle of Enhanced Link Detection also for FX PHYs. One possible solution is to use the Enhanced Link Detection logic inside the ESC, and another possible solution is to implement enhanced link detection logic with external logic, e.g. a CPLD.

The preferred solution is to let the ESC count the RX_ERR of the PHY, and to detect the restart auto-negotiation request of the ESC by some additional logic (CPLD or µController etc.) attached to the MII management interface. This logic should reset the PHY and the Transceiver (power-down) for a short time. This reset causes a link down, which will be detected by the local ESC (which will leave its potential dead-lock state), and by the communication partner (link down, loop closed). If this solution is chosen, Enhanced Link Detection can be enabled in the EEPROM.

The MII management interface is still connected to the PHY, the CPLD/µC just snoops the bus. It is possible to use one CPLD/µC for all ports of the ESC. The PHY address has to be evaluated and individual reset outputs for each PHY have to be used.

Take care that a reset coming from the ESC also turns at least the transceiver off, in order to enable the communication partner to close the loop.

NOTE: Some PHYs use the “signal detect” input to switch into FX operation mode. If the transceiver is powered down, the PHY might not enter FX mode correctly. Other PHYs might not properly keep the auto-negotiation feature turned off, especially as the ESC tries to enable it with the auto-negotiation restart command. In such a case the PHY is required to be put into reset or power-down state, too.

2.7.2.2.1 Proposed solutions with Enhanced Link Detection

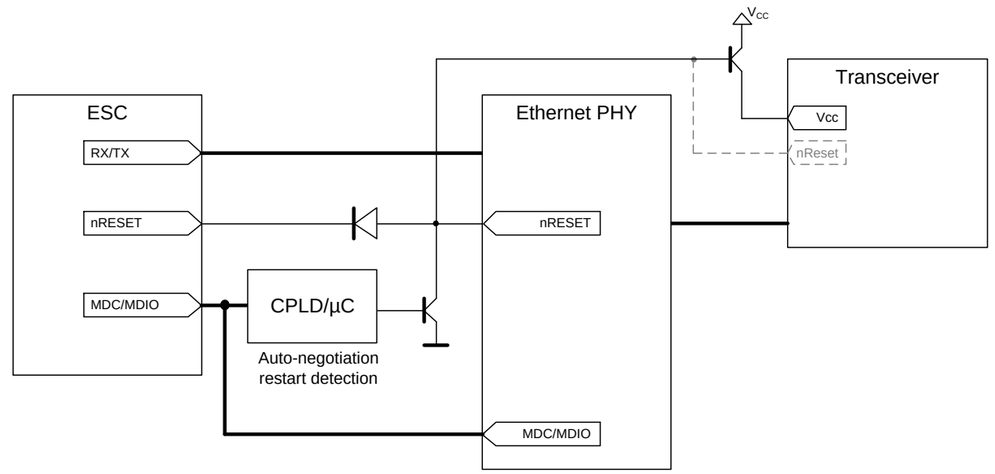

Figure 6: CPLD/µC detects auto-negotiation restart command and resets PHY and transceiver

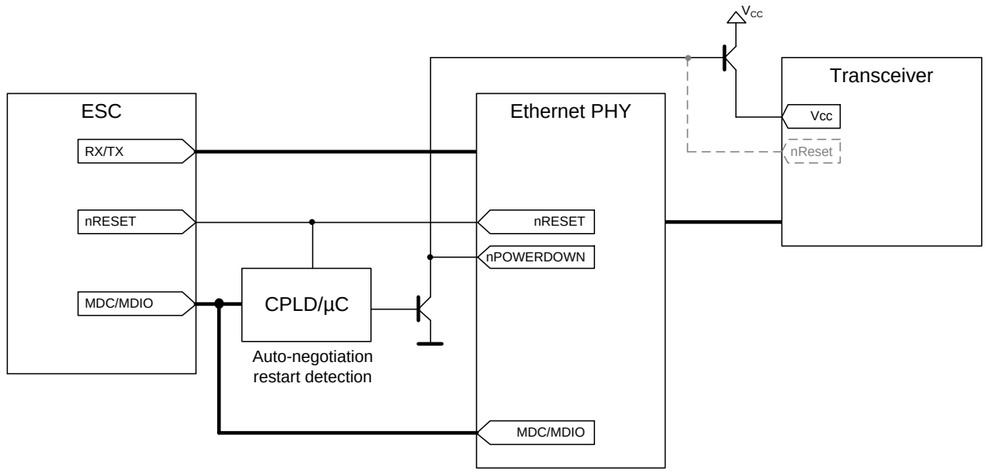

Figure 7: CPLD/µC detects auto-negotiation restart command and powers down PHY and transceiver

NOTE: In Figure 7, the CPLD/µC is connected to the nRESET signal of the ESC/PHY to power-down/reset the transceiver while the ESC/PHY is in reset state.

3 EtherCAT G (1000 Mbit/s)

This chapter is about Ethernet PHYs used for Beckhoff ESCs which support EtherCAT G.

EtherCAT G and Beckhoff ESCs have some general requirements to Ethernet PHYs, which are typically fulfilled by state-of-the-art Ethernet PHYs.

Refer to Section III of the ESC documentation for ESC specific information about supported features.

3.1 Requirements

3.1.1 General requirements

- The PHYs have to comply with **IEEE 802.3**, including
  - The PHYs have to support both **1,000 Mbit/s Full Duplex** and **100 Mbit/s Full Duplex** links.
  - The PHYs have to use autonegotiation.
  - The PHYs have to support the MII management interface.
  - The PHYs have to support MDI/MDI-X auto-crossover.
  - The PHYs must not modify the preamble length.
- The PHYs must not use IEEE802.3az Energy Efficient Ethernet.
- The PHYs must support an additional nibble (odd nibble, dribble nibble) transmitted/received after the FCS in 100Mbit/s operation[12], without marking it with an RX_ER.
- Minimum cable length is 0 m

3.1.2 Additional requirements using Beckhoff ESCs

MAC interface
The PHYs have to provide an **RGMII** interface, including **RGMII In-Band status** signaling (link, speed, duplex).

PHY address
The Beckhoff ESCs use a shared MII Management Interface, so up to 4 different PHY addresses are required. The **PHY addresses 0-3 are recommended**, no address should be used as broadcast/isolate address.

When the PHY does not support addresses 0-3, the specific ESC features must be checked:

- Most ESCs require consecutive PHY addresses, except for the EtherCAT IP Core, which requires up to 3 individual addresses.
- Some ESCs also support a fixed offset, e.g. offset 16 for PHY addresses 16-19, or offset 1 for PHY addresses 1-4. Recommendation is to use offset 16, if that is not possible, offset 1.

PHY configuration
There is not necessarily a µController available in an EtherCAT device, which can configure a PHY. Therefore, PHY configuration must not rely on configuration via the MII management interface, i.e., required features must be enabled after power-on[13], e.g., by default or by **strapping options**.

Only the EtherCAT IP Core supports basic configuration via MII management interface, especially link speed advertisement (MI Link detection and configuration). Any further configuration requires a µController attached to the ESC.

MDC
MII Management interface should not require additional MDC cycles, nor continuous MDC. PHY startup should not rely on MII management interaction, i.e., MDC clocking, since many ESCs do not communicate with the PHY via management interface unless the EtherCAT master requests this.

3.2 Recommendations

- Receive and transmit delays should be deterministic, and as low as possible.
- Maximum cable length should be ≥ 120 m to maintain a safety margin if the standard maximum cable length of 100 m is used.
- RGMII ID (internal delay) should be enabled
- ESD tolerance should be as high as possible (4kV or better)
- Baseline wander at 100Mbit/s should be compensated (the PHYs should cope with the ANSI X3.263 DDJ test pattern for baseline wander measurements at maximum cable length)
- MDC should not incorporate pull-up/pull-down resistors, as this signal is used as a configuration input signal by some ESCs.
- PHY addresses should identify individual PHYs, using address 0-3. A broadcast address, or default isolate address can cause issues with supported PHY addresses.
- Power consumption should be as low as possible.
- I/O voltage: 2.5V/1.8V I/O support is recommended for recent FPGA ESCs.
- Single power supply according to I/O voltage.
- Industrial temperature range should be supported.

[12] SGMII only supports byte transmit/receive, so SGMII is not suitable for EtherCAT G.
[13] This is especially true for: RGMII in-band status enable, EEE disable, preamble/additional nibble maintenance.

3.3 Example PHYs

In this chapter, some example Ethernet PHYs which are assumed to fulfill the EtherCAT requirements are presented, as well as an overview of Ethernet PHYs which are assumed to not fulfill these requirements. These lists represent a current collection of information from data sheets, vendors, and basic hardware tests for some devices, and they represent the best of **current knowledge**. These lists do not imply any kind of certification for EtherCAT G, since none of these PHYs has been tested thoroughly to fulfill each individual EtherCAT G or IEEE802.3 requirement. These lists are only intended for sharing current information about Ethernet PHYs for EtherCAT G, and they are still **work-in-progress**.

The Ethernet PHYs were either judged by a **brief** overview of their data sheets or by additional **basic** hardware communication tests (basic hardware communication tests are indicated in the table).

The example Ethernet PHYs for EtherCAT G shown in the following tables are sorted alphabetically by vendor name, not by preference. The selection of Ethernet PHYs was restricted to 1-4 port 100/1000 Mbit/s Ethernet PHYs. These tables are incomplete in terms of Ethernet PHY vendors and Ethernet PHY devices – they just give some examples, and it is likely that other devices and devices from different vendors meet the requirements as well.

It can not be guaranteed that the mentioned Ethernet PHYs, future revisions of them, or product changes are or will be fully EtherCAT G compatible or not, nor that they are compatible with individual ESCs – because of ESC specific options. As far as known, restrictions and features of the PHYs impacting their EtherCAT G usage are added to the tables.

Table 1 indicates for which ESC the PHY is assumed to be suitable, and which features have to be enabled and which settings have to be made for the ESC/PHY combination.

The main criteria are:

PHY address, PHY address offset
All ESCs support PHY addresses 0-3 for ports 0-3. Future ESCs could support an offset of 16 (using PHY address 16-19), or offset 1 (using PHY address 1-4). The IP core since version 3.0.0 supports independent PHY addresses (including non-consecutive addresses).

RGMII In-Band Status
EtherCAT G ESCs require RGMII In-Band Status for link detection and link speed detection. It must be enabled by default, by strapping, or using an additional µController, which enables this feature in the PHY using the PHY management interface.

EEE (Energy Efficient Ethernet)
EtherCAT G cannot use EEE, thus advertisement and usage have to be disabled. It must be disabled by default, by strapping, or using an additional µController, which disables this feature in the PHY using the PHY management interface.

3.3.1 Example PHYs compatible with EtherCAT G

Table 5: Example Ethernet PHYs assumed to fulfill EtherCAT G requirements

Vendor / Device	# Ports	Basic HW test[14]	PHY addr.[15]	PHY addr. offset[16]	RGMII In-Band Status enable	EEE disable	Comments
Analog Devices							
ADIN1300	1	yes	0-15	0			
Broadcom							
B50212E	1	yes	0,1,24,25	0	µC/MI required	µC/MI required	
BCM54210 BCM54210S BCM54210SE	1		0,1,8,9,16,17,24,25	0	µC/MI required		
BCM54210E	1		0, 1, 24, 25	0	µC/MI required	µC/MI required	
BCM54210PE	1		0-3	0	µC/MI required	µC/MI required	
BCM54214E	1		0-3	0	µC/MI required	µC/MI required	
BCM54216E	1		0-3	0	µC/MI required	µC/MI required	
BCM54220 BCM54220S	2		0-31	0	µC/MI required		
IC Plus Corp.							
IP1001C	1		0-7	0	µC/MI required		
Marvell							
88E1111	1	yes	0-31	0			
88E1510	1		0-1	0			
88E1510P 88E1510Q	1		0-15	0			
88E1512	1		0-1	0			
88E1512P	1		0-15	0			
88E1518	1		0-1				
MaxLinear							
MxL86110	1		1-7	1			PHY address 0 = broadcast
MxL86111	1		1-7	1			PHY address 0 = broadcast

[14] Hardware tests are typically performed with only one of the ESC types, e.g., IP Core. Hardware tests only check basic communication.
[15] PHY address range supported by PHY. Special PHY addresses are excluded (Broadcast/Isolate/Power down).
[16] Suggested PHY address offset. A PHY address offset of 0 means PHY addresses 0-3 are used, an offset of 16 means PHY addresses 16-19 are used, etc..

Vendor / Device	# Ports	Basic HW test[14]	PHY addr.[15]	PHY addr. offset[16]	RGMII In-Band Status enable	EEE disable	Comments
Microchip							
KSZ9031RNX	1		0-7	0			
KSZ9131RNX	1		0-7	0		µC/MI required	
LAN8820	1		0-7	0			
LAN8830	1		0-7	0		Strapping	
LAN8831	1		0-31	0		Strapping	
LAN8840	1		0-7	0		Strapping	
LAN8841	1		0-31	0		Strapping	
Realtek							
RTL8211F	1		1-7	1		µC/MI required	PHY address 0 = broadcast.
RTL8211FS	1		1-7	1		µC/MI required	PHY address 0 = broadcast.
Texas Instruments							
DP83867CR DP83867IRRGZ	1		0-15	0			
DP83867IR	1		0-31	0			
DP83867CS DP83867IS DP83867E	1		0-15	0			
DP83869HM	1		0-15	0			

3.4 PHY Connection

3.4.1 Required Ethernet PHY signals

Table 6: Required Ethernet PHY signals using RGMII

Signal	Required	Comment
RX_CLK	Mandatory	
RX_CTL	Mandatory	
RXD[3:0]	Mandatory	Mandatory: RGMII In-band status for fast link loss reaction time
TX_CLK	Mandatory	
TX_CTL	Mandatory	
TXD[3:0]	Mandatory	
MDIO	Optional	Recommended especially for configuration and debugging
MDC	Optional	Recommended especially for configuration and debugging

3.5 Clock supply

The initial accuracy at room temperature of the PHY clock source has to be 25 ppm or better. This enables FIFO size reduction, i.e., forwarding delay reduction, and supports fast DC locking.

4 Appendix

4.1 Support and service

Beckhoff and our partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

4.1.1 Beckhoff’s branch offices and representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products!

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You will also find further documentation for Beckhoff components there.

4.2 Beckhoff headquarters

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