

Application Note

EtherCAT[®] Slave Controller

Section I – Technology
(Online at <http://www.beckhoff.com>)

Section II – Register Description
(Online at <http://www.beckhoff.com>)

Section III – Hardware Description
(Online at <http://www.beckhoff.com>)

Application Note – ESC Comparison
Feature and register comparison

DOCUMENT ORGANIZATION

The Beckhoff EtherCAT Slave Controller (ESC) documentation covers the following Beckhoff ESCs:

- ET1200
- ET1100
- EtherCAT IP Core for Intel® FPGAs
- EtherCAT IP Core for Xilinx® FPGAs
- ESC20

The documentation is organized in three sections. Section I and section II are common for all Beckhoff ESCs, Section III is specific for each ESC variant.

The latest documentation is available at the Beckhoff homepage (<http://www.beckhoff.com>).

Section I – Technology (All ESCs)

Section I deals with the basic EtherCAT technology. Starting with the EtherCAT protocol itself, the frame processing inside EtherCAT slaves is described. The features and interfaces of the physical layer with its two alternatives Ethernet and EBUS are explained afterwards. Finally, the details of the functional units of an ESC like FMMU, SyncManager, Distributed Clocks, Slave Information Interface, Interrupts, Watchdogs, and so on, are described.

Since Section I is common for all Beckhoff ESCs, it might describe features which are not available in a specific ESC. Refer to the feature details overview in Section III of a specific ESC to find out which features are available.

Section II – Register Description (All ESCs)

Section II contains detailed information about all ESC registers. This section is also common for all Beckhoff ESCs, thus registers, register bits, or features are described which might not be available in a specific ESC. Refer to the register overview and to the feature details overview in Section III of a specific ESC to find out which registers and features are available.

Section III – Hardware Description (Specific ESC)

Section III is ESC specific and contains detailed information about the ESC features, implemented registers, configuration, interfaces, pinout, usage, electrical and mechanical specification, and so on. Especially the Process Data Interfaces (PDI) supported by the ESC are part of this section.

Additional Documentation

Application notes and utilities can also be found at the Beckhoff homepage. Pinout configuration tools for ET1100/ET1200 are available. Additional information on EtherCAT IP Cores with latest updates regarding design flow compatibility, FPGA device support and known issues are also available.

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Patent Pending

The EtherCAT Technology is covered, including but not limited to the following German patent applications and patents: DE10304637, DE102004044764, DE102005009224, DE102007017835 with corresponding applications or registrations in various other countries.

Disclaimer

The documentation has been prepared with care. The products described are, however, constantly under development. For that reason the documentation is not in every case checked for consistency with performance data, standards or other characteristics. In the event that it contains technical or editorial errors, we retain the right to make alterations at any time and without warning. No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

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DOCUMENT HISTORY

Version	Comment
1.0	Initial release
1.1	<ul style="list-style-type: none"> • EtherCAT mode and slave category added • Enhanced Link Detection compatibility added • Editorial changes
1.2	<ul style="list-style-type: none"> • Different versions of ESCs added to comparison • Update to EtherCAT IP Core Release V2.2.0/V2.02a • ESC DL Control register address corrected • ET1100: Register 0x0980 is only available if DC Sync Unit is enabled (0x0140.10=1) • IP Cores: Physical Read/Write Offset (0x0108:0x0109) is configurable • ESC10 removed • Editorial changes
1.3	<ul style="list-style-type: none"> • Added EtherCAT IP Core for Altera FPGAs V2.2.1 • Editorial changes
1.4	<ul style="list-style-type: none"> • Update to ET1100-0002 and ET1200-0002 • Editorial changes
1.5	<ul style="list-style-type: none"> • Update to EtherCAT IP Core for Altera FPGAs V2.3.0, Update to EtherCAT IP Core for Xilinx FPGAs V2.03a • Editorial changes
1.6	<ul style="list-style-type: none"> • Update to EtherCAT IP Core for Altera FPGAs V2.3.1, Update to EtherCAT IP Core for Xilinx FPGAs V2.03b
1.7	<ul style="list-style-type: none"> • Removed Enhanced Link Detection EBUS support for ET1100/ET1200 • Update to EtherCAT IP Core for Altera FPGAs V2.3.2, Update to EtherCAT IP Core for Xilinx FPGAs V2.03c
1.8	<ul style="list-style-type: none"> • Update to EtherCAT IP Core for Altera FPGAs V2.4.0, Update to EtherCAT IP Core for Xilinx FPGAs V2.04a • Added optional LED features • Added FPGA design tool compatibility
1.9	<ul style="list-style-type: none"> • Updated FPGA design tool compatibility
2.0	<ul style="list-style-type: none"> • Update to EtherCAT IP Core for Altera FPGAs V3.0.2, Update to EtherCAT IP Core for Xilinx FPGAs V3.00c • Update to ET1100-0003 and ET1200-0003 • Removed FPGA design tool compatibility (moved to Data sheet addendum)
2.1	<ul style="list-style-type: none"> • Update to EtherCAT IP Core for Altera FPGAs V2.4.3, Update to EtherCAT IP Core for Xilinx FPGAs V2.04d
2.2	<ul style="list-style-type: none"> • Update to EtherCAT IP Core for Altera FPGAs V3.0.5, Update to EtherCAT IP Core for Xilinx FPGAs V3.00f
2.3	<ul style="list-style-type: none"> • Update to EtherCAT IP Core for Altera FPGAs V3.0.6, Update to EtherCAT IP Core for Xilinx FPGAs V3.00g
2.4	<ul style="list-style-type: none"> • Editorial changes
2.5	<ul style="list-style-type: none"> • Update to EtherCAT IP Core for Altera FPGAs V3.0.9, Update to EtherCAT IP Core for Xilinx FPGAs V3.00j
2.6	<ul style="list-style-type: none"> • Update to EtherCAT IP Core for Altera FPGAs V2.4.4 and V3.0.10, Update to EtherCAT IP Core for Xilinx FPGAs V2.04e and V3.00k
2.7	<ul style="list-style-type: none"> • Added IP Core option names to register table, revised Distributed Clocks alternatives • Altera is now Intel • Editorial changes

1 Overview

This application note provides an overview of the features and available registers of the following Beckhoff EtherCAT Slave Controllers:

- ET1200-0003
- ET1100-0003
- EtherCAT IP Core for Intel® FPGAs (up to V2.4.4/V3.0.10)
- EtherCAT IP Core for Xilinx® FPGAs (up to V2.04e/V3.00k)
- ESC20 (Build 22)

Refer to the ESC data sheets for further information. The ESC data sheets are available from the Beckhoff homepage (<http://www.beckhoff.com>).

Table 1: ESC Main Features

Feature	ET1200	ET1100	IP Core (latest)	ESC20
Ports	2-3 (each EBUS/MII, max. 1xMII)	2-4 (each EBUS/MII)	1-3 MII or 1-3 RGMII or 1-2 RMI	2 MII
FMMUs	3	8	0-8	4
SyncManagers	4	8	0-8	4
RAM [Kbyte]	1	8	0-60	4
Distributed Clocks	64 bit	64 bit	32/64 bit	32 bit
Digital I/O	16 bit	32 bit	8-32 bit	32 bit
SPI Slave	Yes	Yes	Yes	Yes
8/16 bit μ Controller	-	Async/Sync	Async	Async
On-chip bus	-	-	Avalon® AMBA® AXI3™ PLB AMBA AXI4™ AMBA AXI4 LITE™	-

2 ESC Features

Table 2: ESC Features

Feature	ET1200-0003	ET1100-0003	IP Core Intel® V3.0.10	IP Core Intel® V3.0.0-3.0.9	IP Core Intel® V2.4.4	IP Core Intel® V2.4.3	IP Core Intel® V2.4.0	IP Core Intel V2.3.1/V2.3.2	IP Core Intel V2.3.0	IP Core Intel V2.2.1	IP Core Intel V2.2.0	IP Core Intel V2.0.0	IP Core Intel V1.1.1	IP Core Intel V1.1.0	IP Core Intel V1.0.0	IP Core Xilinx® V3.00k	IP Core Xilinx® V3.00c-3.00j	IP Core Xilinx® V2.04e	IP Core Xilinx V2.04d	IP Core Xilinx V2.04a	IP Core Xilinx V2.03d	IP Core Xilinx V2.03b/c	IP Core Xilinx V2.03a	IP Core Xilinx V2.02a	IP Core Xilinx V2.00a	IP Core Xilinx V1.01b	ESC20	
EtherCAT Ports	2-3	2-4	1-3	1-3	1-3	1-3	1-3	1-3	1-3	2-3	2-3	2	2	2	2	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	2	2	2
Permanent ports	2	2-4	1-3	1-3	1-3	1-3	1-3	1-3	1-3	2-3	2-3	2	2	2	2	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	2	2	2	
Optional Bridge port 3 (EBUS or MII)	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
EBUS ports	1-3	0-4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
MII ports	0-1	0-4	0-3	0-3	0-3	0-3	0-3	0-3	0-3	0/2/3	0/2/3	0/2	0/2	0/2	0/2	0-3	0-3	0-3	0-3	0-3	0-3	0-3	0-3	0-3	0-3	0/2	0/2	2
RMI ports	-	-	0-2	0-2	0-2	0-2	0-2	0-2	0-2	0/2	0/2	0/2	0/2	0/2	0/2	0-2	0-2	0-2	0-2	0-2	0-2	0-2	0-2	0-2	0/2	0/2	0/2	-
RGMI ports	-	-	0-3	0-3	-	-	-	-	-	-	-	-	-	-	-	0-3	0-3	-	-	-	-	-	-	-	-	-	-	
Port 0	-	-	x	x	x	x	x	x	x	-	-	-	-	-	-	x	x	x	x	x	x	x	x	x	-	-	-	
Ports 0, 1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Ports 0, 1, 2	-	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	x	-	-	-	
Ports 0, 1, 3	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Ports 0, 1, 2, 3	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
EtherCAT mode	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	
Slave Category	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	Full Slave	
Position addressing	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Node addressing	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Logical addressing	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Broadcast addressing	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Physical Layer General Features																												
FIFO Size configurable (0x0100[18:16])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
FIFO Size default from SII EEPROM	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Auto-Forwarder checks CRC and SOF	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Forwarded RX Error indication, detection and Counter (0x0308:0x030B)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Lost Link Counter (0x0310:0x0313)	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	
Prevention of circulating frames	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Fallback: Port 0 opens if all ports are closed	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
VLAN Tag and IP/UDP support	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Enhanced Link Detection per port configurable	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
EBUS Features																												
Low Jitter	x	x																										
Enhanced Link Detection supported	-	-																										
Enhanced Link Detection compatible	x	x																										
EBUS signal validation	x	x																										
LVDS Transceiver internal	x	x																										
LVDS sample rate [MHz]	1,000	1,000																										
Remote link down signaling time configurable 0x0100[22]	x	x																										

Feature	ET1200-0003	ET1100-0003	IP Core Intel® V3.0.10	IP Core Intel® V3.0.0-3.0.9	IP Core Intel® V2.4.4	IP Core Intel® V2.4.3	IP Core Intel® V2.4.0	IP Core Intel V2.3.1/V2.3.2	IP Core Intel V2.3.0	IP Core Intel V2.2.1	IP Core Intel V2.2.0	IP Core Intel V2.0.0	IP Core Intel V1.1.1	IP Core Intel V1.1.0	IP Core Intel V1.0.0	IP Core Xilinx® V3.00k	IP Core Xilinx® V2.04e	IP Core Xilinx V2.04d	IP Core Xilinx V2.04a	IP Core Xilinx V2.03d	IP Core Xilinx V2.03b/c	IP Core Xilinx V2.03a	IP Core Xilinx V2.02a	IP Core Xilinx V2.00a	IP Core Xilinx V1.01b	ESC20	
General Ethernet Features (MI/RMI/RGMII)																											
MII Management Interface (0x0510:0x051F)	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
Supported PHY Address Offsets	0/16	0/16	any	any	any	any	any	any	any	any	any	any	0/16	0/16	0/16	any	any	any	any	any	any	any	any	any	any	0/16	0
Individual port PHY addresses	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-
Port PHY addresses readable	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-
Link Polarity configurable	-	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	-
Enhanced Link Detection supported	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-
FX PHY support (native)	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-
PHY reset out signals	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-
Link detection using PHY signal (LED)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MI link status and configuration	-	-	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	-	-	-	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	-
MI controllable by PDI (0x0516:0x0517)	-	-	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-
MI read error (0x0510[13])	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-
MI PHY configuration update status (0x0518[5])	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	
MI preamble suppression	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	
Additional MCLK	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	
Gigabit PHY configuration	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	
Gigabit PHY register 9 detection	-	-	relaxed	relaxed	relaxed	relaxed	-	-	-	-	-	-	-	-	-	relaxed	relaxed	relaxed	relaxed	-	-	-	-	-	-	-	
FX PHY configuration	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	
Transparent Mode	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
MII Features																											
CLK25OUT as PHY clock source	x	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	-
Bootstrap TX Shift settings	x	x	c	c	c	c	c	c	c	c	c	c	User logic	User logic	User logic	c	c	c	c	c	c	c	c	c	c	-	-
Automatic TX Shift setting (with TX_CLK)	-	-	c	c	c	c	c	c	c	c	c	c	-	-	-	c	c	c	c	c	c	c	c	c	c	-	
TX Shift not necessary (PHY TX_CLK as clock source)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x	
FIFO size reduction steps	1	1	2	2	1	1	1	1	1	1	1	1	1	1	1	2	2	1	1	1	1	1	1	1	1	1	
PDI General Features																											
Increased PDI performance	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	
Extended PDI Configuration (0x0152:0x0153)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
PDI Error Counter (0x030D)	-	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-	
PDI Error Code (0x030E)	-	-	c	c	c	c	c	c	c	c	c	c	-	-	-	c	c	c	c	c	c	c	c	c	c	-	
CPU_CLK output (10, 20, 25 MHz)	x	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	-
SOF, EOF, WD_TRIG and WD_STATE independent of PDI	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	
Available PDIs and PDI features depending on port configuration	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
PDI selection at run-time (SII EEPROM)	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x	
PDI active immediately (SII EEPROM settings ignored)	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	
PDI function acknowledge by write	-	-	c	c	-	-	-	-	-	-	-	-	-	-	-	c	c	-	-	-	-	-	-	-	-	-	
PDI Information register 0x014E:0x014F	-	-	c	c	-	-	-	-	-	-	-	-	-	-	-	c	c	-	-	-	-	-	-	-	-	-	

Feature	ET1200-0003	ET1100-0003	IP Core Intel® V3.0.10	IP Core Intel® V3.0.0-3.0.9	IP Core Intel® V2.4.4	IP Core Intel® V2.4.3	IP Core Intel® V2.4.0	IP Core Intel V2.3.1/V2.3.2	IP Core Intel V2.3.0	IP Core Intel V2.2.1	IP Core Intel V2.2.0	IP Core Intel V2.0.0	IP Core Intel V1.1.1	IP Core Intel V1.1.0	IP Core Intel V1.0.0	IP Core Xilinx® V3.00k	IP Core Xilinx® V2.04e	IP Core Xilinx V2.04d	IP Core Xilinx V2.04a	IP Core Xilinx V2.03d	IP Core Xilinx V2.03b/c	IP Core Xilinx V2.03a	IP Core Xilinx V2.02a	IP Core Xilinx V2.00a	IP Core Xilinx V1.01b	ESC20
Digital I/O PDI	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Digital I/O width [bits]	8/16	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	32
PDI Control register value (0x0140:0x0141)	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	16-20
Control/Status signals:	2/0 ^{1,2}	7/0 ²	7	7	7	7	7	7	7	7	7	7	5	5	5	7	7	7	7	7	7	7	7	7	5	-
LATCH_IN	x ^{1,2}	x ²	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
SOE	x ^{1,2}	x ²	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
OUTVALID	x ^{1,2}	x ²	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
WD_TRIG	x ^{1,2}	x ²	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
OE_CONF	-	x ²	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
OE_EXT	-	x ²	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
EEPROM_Loaded	-	x ²	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-
WD_STATE	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	-	-
EOF	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	-	-
Granularity of direction configuration [bits]	2	2	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
Bidirectional mode	x	x	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	-
Output high-Z if WD expired	x	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	-
Output 0 if WD expired	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Output with EOF	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Output with DC SyncSignals	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Input with SOE	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Input with DC SyncSignals	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
SPI Slave PDI	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Max. SPI clock [MHz]	6-20 (SPI mode dep.)	20	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	15
SPI modes configurable (0x0150[1:0])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
SPI_IRQ driver configurable (0x0150[3:2])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
SPI_SEL polarity configurable (0x0150[4])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Data out sample mode configurable (0x0150[5])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Busy signaling	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x
Wait State byte(s)	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Number of address extension byte(s)	1	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	-
2/4 Byte SPI master support	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Extended error detection (read busy violation)	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
SPI_IRQ delay	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Status indication	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
EEPROM_Loaded signal	x	x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-

¹ Shared control/status signals: LATCH_IN/SOE and OUT_VALID/WD_TRIGGER

² Availability depending on port configuration

Feature	ET1200 -0003	ET1100 -0003	IP Core Intel® V3.0.10	IP Core Intel® V3.0.0- 3.0.9	IP Core Intel® V2.4.4	IP Core Intel® V2.4.3	IP Core Intel® V2.4.0	IP Core Intel V2.3.1/ V2.3.2	IP Core Intel V2.3.0	IP Core Intel V2.2.1	IP Core Intel V2.2.0	IP Core Intel V2.0.0	IP Core Intel V1.1.1	IP Core Intel V1.1.0	IP Core Intel V1.0.0	IP Core Xilinx® V3.00k	IP Core Xilinx® V2.04e	IP Core Xilinx V2.04d	IP Core Xilinx V2.04a	IP Core Xilinx V2.03d	IP Core Xilinx V2.03b/c	IP Core Xilinx V2.03a	IP Core Xilinx V2.02a	IP Core Xilinx V2.00a	IP Core Xilinx V1.01b	ESC20
Asynchronous μController PDI	-	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit
Extended μC configuration bits (0x0150[7:4], 0x0152:0x0153)		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
ADR[15:13] available (000b if not available)		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
EEPROM_Loaded signal		x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-
RD polarity configurable (0x0150[7])		x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Read BUSY delay (0x0152[0])		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Write after first edge (0x0152[2])		-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Default BUSY state		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Synchronous μController PDI	-	8/16 bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EEPROM_Loaded signal		x																								
On-Chip Bus PDI	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Avalon®			x	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	-	-	-	-	-	-	-	-
OPB®			-	-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x	x	x	x	x	-
PLB v4.6®			-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x	x	x	x	x	x	-
AXI3™			x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
AXI4™			-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-
AXI4 LITE™			-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-
Bus clock [MHz] (N=1,2,3,...)			any	any	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25	25	any	any	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25
Data bus width [bits]			8/16/32/64	8/16/32/64	8	8	8	8	8	8	8	8	8	8	8	8/16/32/64	8/16/32/64	32	32	32	32	32	32	32	32	32
Prefetch cycles			1	1	1/2/4	1/2/4	1/2/4	1/2/4	1/2/4	1/2/4	1/2/4	1/2/4	1/2/4	4	4	1	1	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4 (OPB)	4
DC SyncSignals available directly and as IRQ			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Bus clock multiplier in register 0x0150[6:0]			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
EEPROM_Loaded signal			x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-
EtherCAT Bridge (port 3, EBUS/MI)	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
General Purpose I/O	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
GPO bits	0-12	0-16	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64
GPI bits	-	0-16	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64
GPIO available independent of PDI or port configuration		-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
GPIO available without PDI		-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Concurrent access to GPO by ECAT and PDI		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
ESC Information																										
Basic Information (0x0000:0x0006)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Port Descriptor (0x0007)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
ESC Features supported (0x0008:0x0009)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Extended ESC Feature Availability in User RAM (0x0F80 ff.)	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Write Protection (0x0020:0x0031)	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x

Feature	ET1200-0003	ET1100-0003	IP Core Intel® V3.0.10	IP Core Intel® V3.0.0-3.0.9	IP Core Intel® V2.4.4	IP Core Intel® V2.4.3	IP Core Intel® V2.4.0	IP Core Intel V2.3.1/V2.3.2	IP Core Intel V2.3.0	IP Core Intel V2.2.1	IP Core Intel V2.2.0	IP Core Intel V2.0.0	IP Core Intel V1.1.1	IP Core Intel V1.1.0	IP Core Intel V1.0.0	IP Core Xilinx® V3.00k	IP Core Xilinx® V3.00c-3.00j	IP Core Xilinx® V2.04e	IP Core Xilinx V2.04d	IP Core Xilinx V2.04a	IP Core Xilinx V2.03d	IP Core Xilinx V2.03b/c	IP Core Xilinx V2.03a	IP Core Xilinx V2.02a	IP Core Xilinx V2.00a	IP Core Xilinx V1.01b	ESC20	
Data Link Layer Features																												
ECAT Reset (0x0040)	x	x	c	c	c	c	c	c	c	c	c	c	-	-	-	-	c	c	c	c	c	c	c	c	c	-	-	-
PDI Reset (0x0041)	-	-	c	c	c	c	c	c	c	c	c	c	-	-	-	-	c	c	c	c	c	c	c	c	c	-	-	-
ESC DL Control (0x0100:0x0103) bytes	4	4	4	4	4	4	4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2	4	4	4	4	4	4	2/4	2/4	2/4	2/4	2/4	2/4	4
EtherCAT only mode (0x0100[0])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Temporary loop control (0x0100[1])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	
FIFO Size configurable (0x0100[18:16])	x	x	x	x	x	x	x	c	c	c	c	c	c	c	c	x	x	x	x	x	x	c	c	c	c	c	x	
Configured Station Address (0x0010:0x0011)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Configured Station Alias (0x0100[24], 0x0012:0x0013)	x	x	x	x	x	x	x	c	c	c	c	c	c	c	c	x	x	x	x	x	c	c	c	c	c	c	x	
Physical Read/Write Offset (0x0108:0x0109)	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x	
Application Layer Features																												
Extended AL Control/Status bits (0x0120[15:5], 0x0130[15:5])	x	x	x	x	x	x	x	-	-	-	-	-	-	-	-	x	x	x	x	x	-	-	-	-	-	-	-	
AL Status Emulation (0x0140[8])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
AL Status Code (0x0134:0x0135)	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x	
Interrupts																												
ECAT Event Mask (0x0200:0x0201)	x	x	x	x	x	x	x	c	c	c	c	c	c	c	c	x	x	x	x	x	c	c	c	c	c	c	x	
AL Event Mask (0x0204:0x0207)	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x	
ECAT Event Request (0x0210:0x0211)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
AL Event Request (0x0220:0x0223)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
SyncManager activation changed (0x0220[4])	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	x	
SyncManager watchdog expiration (0x0220[6])	-	-	x	x	x	x	x	x	x	-	-	-	-	-	-	x	x	x	x	x	x	x	x	-	-	-	-	
Error Counters																												
RX Error Counter (0x0300:0x0307)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Forwarded RX Error Counter (0x0308:0x030B)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	
ECAT Processing Unit Error Counter (0x030C)	-	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-	
PDI Error Counter (0x030D)	-	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-	
Lost Link Counter (0x0310:0x0313)	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x	
Watchdog																												
Watchdog Divider configurable (0x0400:0x0401)	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x	
Watchdog Process Data	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Watchdog PDI	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
Watchdog Counter Process Data (0x0442)	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-	
Watchdog Counter PDI (0x0443)	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-	

Feature	ET1200-0003	ET1100-0003	IP Core Intel® V3.0.10	IP Core Intel® V3.0.0-3.0.9	IP Core Intel® V2.4.4	IP Core Intel® V2.4.3	IP Core Intel® V2.4.0	IP Core Intel V2.3.1/V2.3.2	IP Core Intel V2.3.0	IP Core Intel V2.2.1	IP Core Intel V2.2.0	IP Core Intel V2.0.0	IP Core Intel V1.1.1	IP Core Intel V1.1.0	IP Core Intel V1.0.0	IP Core Xilinx® V3.00k	IP Core Xilinx® V2.04e	IP Core Xilinx V2.04d	IP Core Xilinx V2.04a	IP Core Xilinx V2.03d	IP Core Xilinx V2.03b/c	IP Core Xilinx V2.03a	IP Core Xilinx V2.02a	IP Core Xilinx V2.00a	IP Core Xilinx V1.01b	ESC20	
SII EEPROM Interface (0x0500:0x050F)																											
EEPROM sizes supported	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	16 Kbyte-4 Mbyte	16 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	1 Kbyte-4 Mbyte	16 Kbyte-4 Mbyte
EEPROM size reflected in 0x0502[7]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
EEPROM controllable by PDI	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
EEPROM Emulation by PDI	-	-	c	c	c	c	c	c	c	c	c	c	c	-	-	-	c	c	c	c	c	c	c	c	c	c	-
EEPROM Emulation CRC error 0x0502[11] PDI writable	-	-	x	-	x	x	x	x	x	x	x	x	-	-	-	x	-	x	x	x	x	x	x	x	x	-	-
Read data bytes (0x0502[6])	8	8	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
Internal Pull-Ups for EEPROM_CLK and EEPROM_DATA	x	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	-
I2C base address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FMUs	3	8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	4
Bit-oriented operation	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
SyncManagers	4	8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	4
Watchdog trigger generation for 1 Byte Mailbox configuration independent of reading access	x	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-
SyncManager Event Times (+0x8[7:6])	-	x	c	c	c	c	c	c	c	c	c	c	c	c	-	c	c	c	c	c	c	c	c	c	c	c	-
Buffer state (+0x5[7:6])	-	-	x	x	x	x	x	x	x	x	x	x	x	-	-	x	x	x	x	x	x	x	x	x	x	x	-
SyncManager Sequential mode	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SyncManager deactivation delay	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Distributed Clocks	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
Width	64	64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32	32	32	32	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32	32
Sync/Latch signals	1-2 ³	2	4 (0-2 Sync-Signals, 0-2 Latch-Signals)	4 (0-2 Sync-Signals, 0-2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (0-2 Sync-Signals, 0-2 Latch-Signals)	4 (0-2 Sync-Signals, 0-2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	2
SyncManager Event Times (0x09F0:0x09FF)	-	x	c	c	c	c	c	c	c	c	c	c	c	c	-	c	c	c	c	c	c	c	c	c	c	c	-
DC Receive Times	x	x	c	c	c	c	c	c	c	c	c	c	if DC on	if DC on	if DC on	if DC on	c	c	c	c	c	c	c	c	c	c	x
DC Time Loop Control controllable by PDI	-	-	c	c	c	c	c	c	c	c	c	c	c	-	-	-	c	c	c	c	c	c	c	c	c	c	-
DC Sync/Latch activation (0x0140[11:10])	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Propagation delay measurement with traffic (BWR/FPWR 0x900 detected at each port)	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
LatchSignal state in Latch Status register (0x09AE:0x09AF)	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
SyncSignal Auto-Activation (0x0981[3])	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	
SyncSignal 32 or 64 bit Start Time (0x0981[4])	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	
SyncSignal Late Activation (0x0981[6:5])	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	
SyncSignal debug pulse (0x0981[7])	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	
SyncSignal Activation State 0x0984	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	
Reset filters after writing filter depth	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	

³ SYNC/LATCH[1] available if no MII port is used.

Feature	ET1200-0003	ET1100-0003	IP Core Intel® V3.0.10	IP Core Intel® V3.0.0-3.0.9	IP Core Intel® V2.4.4	IP Core Intel® V2.4.3	IP Core Intel® V2.4.0	IP Core Intel V2.3.1/V2.3.2	IP Core Intel V2.3.0	IP Core Intel V2.2.1	IP Core Intel V2.2.0	IP Core Intel V2.0.0	IP Core Intel V1.1.1	IP Core Intel V1.1.0	IP Core Intel V1.0.0	IP Core Xilinx® V3.00k	IP Core Xilinx® V2.04e	IP Core Xilinx V2.04d	IP Core Xilinx V2.04a	IP Core Xilinx V2.03d	IP Core Xilinx V2.03b/c	IP Core Xilinx V2.03a	IP Core Xilinx V2.02a	IP Core Xilinx V2.00a	IP Core Xilinx V1.01b	ESC20			
ESC Specific Registers (0x0E00:0x0EFF)																													
Product and Vendor ID	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-		
POR Values	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
FPGA Update (online)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x		
Process RAM and User RAM																													
Process RAM (0x1000 ff.) [Kbyte]	1	8	0-60	0-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	0-60	0-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	4	
User RAM (0x0F80:0x0FFF)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
Extended ESC Feature Availability in User RAM	-	-	x	x	x	x	x	x	x	x	x	x	x	x	-	x	x	x	x	x	x	x	x	x	x	x	-		
RAM initialization	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
Additional EEPROMs																													
SII EEPROM (iPC)	x	x	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	^c (EEPROM of μC used)	x	x
FPGA configuration EEPROM	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
LED Signals																													
RUN LED	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x	
RUN LED override	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-		
Link/Activity(x) LED per port	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
PERR(x) LED per port	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
Device ERR LED	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-		
STATE_RUN LED	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-		
Optional LED states																													
RUN LED: Bootstrap	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
RUN LED: Booting	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-		
RUN LED: Device identification	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-		
RUN LED: loading SII EEPROM	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-		
Error LED: SII EEPROM loading error	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-		
Error LED: Invalid hardware configuration	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
Error LED: Process data watchdog timeout	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-		
Error LED: PDI watchdog timeout	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-		
Error LED: Error Indication 0x0130[4]	-	-	c	c	-	-	-	-	-	-	-	-	-	-	-	c	c	-	-	-	-	-	-	-	-	-	-		
Link/Activity: port closed	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
Link/Activity: local auto-negotiation error	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
Link/Activity: remote auto-negotiation error	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
Link/Activity: unknown PHY auto-negotiation error	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
LED test	-	-	c	c	-	-	-	-	-	-	-	-	-	-	-	c	c	-	-	-	-	-	-	-	-	-	-		
Clock supply																													
Crystal	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
Crystal oscillator	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-		
TX_CLK from PHY	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
25ppm clock source accuracy	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
Internal PLL	x	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	x		
Power Supply Voltages																													
3.3 V	x	x	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	x	
3.3V / 5V tolerant	-	-	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	-	
5 V	(x)	(x)	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	-	
Core Voltage																													
Core Voltage	2.5V	2.5V	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	1.5V	
Internal LDOs																													
LDO supply voltage	2	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
Core Voltage	3.3V/5V	3.3V/5V	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
I/O Voltage	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		

Feature	ET1200-0003	ET1100-0003	IP Core Intel® V3.0.10	IP Core Intel® V3.0.0-3.0.9	IP Core Intel® V2.4.4	IP Core Intel® V2.4.3	IP Core Intel® V2.4.0	IP Core Intel V2.3.1/V2.3.2	IP Core Intel V2.3.0	IP Core Intel V2.2.1	IP Core Intel V2.2.0	IP Core Intel V2.0.0	IP Core Intel V1.1.1	IP Core Intel V1.1.0	IP Core Intel V1.0.0	IP Core Xilinx® V3.00k	IP Core Xilinx® V3.00c-3.00j	IP Core Xilinx® V2.04e	IP Core Xilinx V2.04d	IP Core Xilinx V2.04a	IP Core Xilinx V2.03d	IP Core Xilinx V2.03b/c	IP Core Xilinx V2.03a	IP Core Xilinx V2.02a	IP Core Xilinx V2.00a	IP Core Xilinx V1.01b	ESC20
Package	QFN48	BGA128	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	BGA256
Size [mm²]	7x7	10x10	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	17x17
Original Release date	11/2006	3/2007	1/2015	3/2013	1/2015	7/2013	3/2011	2/2010	12/2009	6/2009	6/2008	8/2007	1/2007	11/2006	7/2006	1/2015	5/2013	1/2015	7/2013	3/2011	6/2010	2/2010	12/2009	6/2008	8/2007	1/2007	7/2005
Configuration and Pinout calculator (XLS)	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Register Configuration	fixed	fixed	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	fixed
License device required	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Evaluation version	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Vendor ID package	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Internal tri-state drivers	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
IPCore configuration tool	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-
XPS IP cores	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-
Example designs/ pre-synthesized time-limited evaluation core included in setup	-	-	4/4	6/6	3/3	5/4	5/4	7/3	7/3	7/3	7/3	4/-	4/-	4/-	2/-	3/3	4/3	2/1	4/2	4/2	3/1	3/1	3/1	4/1	3/-	3/-	-
FB1120 Digital I/O	-	-	-	-	-	-	-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	-	-	-	-	-	-	-	-	-	-	-	-
FB1120 SPI	-	-	-	-	-	-	-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	-	-	-	-	-	-	-	-	-	-	-	-
FB1122 Digital I/O	-	-	-	x/x	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-	-	-	-	-	-	-	-	-	-	-	-
FB1122 SPI	-	-	-	x/x	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-	-	-	-	-	-	-	-	-	-	-	-
DBC2C20 Digital I/O	-	-	-	-	-	-	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-	-	-	-	-	-	-	-	-	-	-	-
DBC2C20 NIOS®	-	-	-	-	-	-	-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	-	-	-	-	-	-	-	-	-	-	-	-
DBC3C40 Digital I/O	-	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-	-	-	-	-	-	-	-	-	-	-	-
DBC3C40 NIOS	-	-	-	-	-	-	-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	-	-	-	-	-	-	-	-	-	-	-	-
DBC4CE55 NIOS	-	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-	-	-	-	-	-	-	-	-	-	-	-
DE2-115 NIOS MII	-	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-	-	-	-	-	-	-	-	-	-	-	-
DE2-115 NIOS RGMII	-	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-	-	-	-	-	-	-	-	-	-	-	-
FB1130 Digital I/O	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-
FB1130 SPI	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	-
FB1130 PLB®	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	x/-	-
FB1130 OPB®	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
FB1130 PLB2OPB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LX150T PLB2AXI®	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LX150T Digital I/O	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-
LX150T AXI	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-
ZC702 AXI (PlanAhead)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ZC702 AXI (Vivado)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	x/x	-

Table 3: ESC Feature Legend

Symbol	Description
x	available
-	not available
c	configurable
User logic	Functionality can be added by user logic inside the FPGA
red	Feature changed in this version

3 ESC Registers

Table 4: ESC Registers

Address	Length (Byte)	Description	ET1200	ET1100	IP Core V3.0.0-V3.0.10, V3.00c-V3.00k	IP Core V2.4.0-V2.4.4/V2.04a-V2.04e			IP Core V2.3.0-V2.3.2/V2.03a-V2.03d			IP Core V2.2.1/V2.2.0/V2.02a			IP Core V2.0.0/V2.00a			IP Core V1.1.1/V1.01b			IP Core V1.1.0			IP Core V1.0.0			ESC20	IP Core Option
						Register set			Register set			Register set			Register set			Register set			Register set							
						S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L		
0x0000	1	Type	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0001	1	Revision	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0002:0x0003	2	Build	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0004	1	FMMUs supported	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0005	1	SyncManagers supported	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0006	1	RAM Size	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0007	1	Port Descriptor	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-		
0x0008:0x0009	2	ESC Features supported	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0010:0x0011	2	Configured Station Address	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0012:0x0013	2	Configured Station Alias	x	x	x	x	x	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x		
0x0020	1	Write Register Enable	x	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	Write Protection	
0x0021	1	Write Register Protection	x	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	Write Protection	
0x0030	1	ESC Write Enable	x	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	Write Protection	
0x0031	1	ESC Write Protection	x	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	Write Protection	
0x0040	1	ESC Reset ECAT	x	x	c	c	c	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	-	-	RESET slave by ECAT/PDI	
0x0041	1	ESC Reset PDI	-	-	c	c	c	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	-	-	RESET slave by ECAT/PDI	
0x0100:0x0101	2	ESC DL Control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0102:0x0103	2	Extended ESC DL Control	x	x	x	x	x	r/c	r/c	x	r/c	r/c	x	r/c	r/c	x	r	r	x	r	r	x	r	r	x	x		
0x0108:0x0109	2	Physical Read/Write Offset	x	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	Read/Write Offset	
0x0110:0x0111	2	ESC DL Status	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0120	5 bits [4:0]	AL Control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0120:0x0121	2	AL Control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0130	5 bits [4:0]	AL Status	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0130:0x0131	2	AL Status	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0134:0x0135	2	AL Status Code	x	x	c	c	x	x	c	x	x	c	x	x	c	x	x	-	x	x	-	x	x	-	-	-	x	AL Status Code Register
0x0138	1	RUN LED Override	-	-	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Extended RUN/ERR LED	
0x0139	1	ERR LED Override	-	-	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Extended RUN/ERR LED	
0x0140	1	PDI Control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0141	1	ESC Configuration	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x014E:0x014F	2	PDI Information	-	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PDI Information Register	
0x0150	1	PDI Configuration	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0151	1	DC Sync/Latch Configuration	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			
0x0152:0x0153	2	Extended PDI Configuration	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x			

Address	Length (Byte)	Description	ET1200	ET1100	IP Core V3.0.0-V3.0.10, V3.00c-V3.00k	IP Core V2.4.0-V2.4.4/ V2.04a-V2.04e			IP Core V2.3.0-V2.3.2/ V2.03a-V2.03d			IP Core V2.2.1/V2.2.0/ V2.02a			IP Core V2.0.0/V2.00a			IP Core V1.1.1/V1.01b			IP Core V1.1.0			IP Core V1.0.0			ESC20	IP Core Option
						Register set			Register set			Register set			Register set			Register set			Register set							
						S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L		
0x0200:0x0201	2	ECAT Event Mask	x	x	x	x	x	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	x	
0x0204:0x0207	4	PDI AL Event Mask	x	x	r/c	r/c	x	x	r/c	x	x	r/c	x	x	r/c	x	x	r	x	x	r	x	x	r	x	x	x	AL Event Mask Register
0x0210:0x0211	2	ECAT Event Request	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0220:0x0223	4	AL Event Request	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0300:0x0307	4x2	Rx Error Counter[3:0]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0308:0x030B	4x1	Forwarded Rx Error counter[3:0]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	
0x030C	1	ECAT Processing Unit Error Counter	-	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	-	EPU and PDI Error Counter
0x030D	1	PDI Error Counter	-	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	-	EPU and PDI Error Counter
0x030E	1	PDI Error Code	-	-	c	c	c	x	c	c	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EPU and PDI Error Counter
0x0310:0x0313	4x1	Lost Link Counter[3:0]	x	x	c	c	x	x	c	x	x	c	x	x	c	x	x	-	x	x	-	x	x	-	x	x	x	Lost Link Counter
0x0400:0x0401	2	Watchdog Divider	x	x	r/c	r/c	x	x	r/c	x	x	r/c	x	x	r/c	x	x	r	x	x	r	x	x	r	x	x	x	Extended Watchdog
0x0410:0x0411	2	Watchdog Time PDI	x	x	c	c	x	x	c	x	x	c	x	x	c	x	x	-	x	x	-	x	x	-	x	x	x	Extended Watchdog
0x0420:0x0421	2	Watchdog Time Process Data	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0440:0x0441	2	Watchdog Status Process Data	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0442	1	Watchdog Counter Process Data	x	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	-	Watchdog Counter
0x0443	1	Watchdog Counter PDI	x	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	-	Watchdog Counter
0x0500:0x050F	16	SII EEPROM Interface	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0510:0x0515	6	MII Management Interface	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	-	x	x	-	x	x	-	x	x	x	PHY Management Interface
0x0516:0x0517	2	MII Management Access State	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	PHY Management Interface
0x0518:0x051B	4	PHY Port Status[3:0]	-	-	c	c	c	c	c	c	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	Link state and PHY configuration through MI
0x0600:0x06FC	16x13	FMMU[15:0]	3	8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	4	Number of FMMU
0x0800:0x087F	16x8	SyncManager[15:0]	4	8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	4	Number of SyncManagers

Address	Length (Byte)	Description	ET1200	ET1100	IP Core V3.0.0-V3.0.10, V3.00c-V3.00k	IP Core V2.4.0-V2.4.4/ V2.04a-V2.04e			IP Core V2.3.0-V2.3.2/ V2.03a-V2.03d			IP Core V2.2.1/V2.2.0/ V2.02a			IP Core V2.0.0/V2.00a			IP Core V1.1.1/V1.01b			IP Core V1.1.0			ESC20	IP Core Option			
						Register set			Register set			Register set			Register set			Register set			Register set							
						S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L			S	M	L
0x0900:0x090F	4x4	DC – Receive Times	x	x	RT	RT	RT	RT	RT	RT	RT	RT	RT	RT	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0910:0x0917	8	DC – System Time	x	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0918:0x091F	8	DC – Receive Time EPU	x	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0920:0x0927	8	DC – System Time Offset	x	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0928:0x092B	4	DC – System Time Delay	x	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x092C:0x092F	4	DC – System Time Difference	x	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0930:0x0931	2	DC – Speed Counter Start	x	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0932:0x0933	2	DC – Speed Counter Diff	x	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0934	1	DC – System Time Difference Filter Depth	x	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0935	1	DC – Speed Counter Filter Depth	x	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0936	1	DC – Receive Time Latch mode	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x	
0x0980	1	DC – Cyclic Unit Control	x	S	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0981	1	DC – Activation	x	S	S	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0982:0x0983	2	DC – Pulse length of SyncSignals	x	S	S	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0984	1	DC – Activation Status	-	-	S	DC	DC	DC	DC	DC	DC	DC	DC	DC	-	-	-	-	-	-	-	-	-	-	-	-	-	Refer to legend
0x098E	1	DC – SYNC0 Status	x	S	S0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x098F	1	DC – SYNC1 Status	x	S	S1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0990:0x0997	8	DC – Next Time Cyclic Operation/Next SYNC0 Pulse	x	S	S0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x0998:0x099F	8	DC – Next SYNC1 Pulse	x	S	S1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09A0:0x09A3	4	DC – SYNC0 Cycle Time	x	S	S0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09A4:0x09A7	4	DC – SYNC1 Cycle Time	x	S	S1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09A8	1	DC – Latch0 Control	x	L	L0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09A9	1	DC – Latch1 Control	x	L	L1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09AE	1	DC – Latch0 Status	x	L	L0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09AF	1	DC – Latch1 Status	x	L	L1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09B0:0x09B7	8	DC – Latch0 Positive Edge	x	L	L0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09B8:0x09BF	8	DC – Latch0 Negative Edge	x	L	L0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09C0:0x09C7	8	DC – Latch1 Positive Edge	x	L	L1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09C7:0x09CF	8	DC – Latch1 Negative Edge	x	L	L1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	Refer to legend
0x09F0:0x09F3	4	DC – EtherCAT Buffer Change Event Time	-	SL	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	-	-	DC	-	-	DC	-	-	DC	-	Refer to legend
0x09F8:0x09FB	4	DC – PDI Buffer Start Event Time	-	SL	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	-	-	DC	-	-	DC	-	-	DC	-	Refer to legend
0x09FC:0x09FF	4	DC – PDI Buffer Change Event Time	-	SL	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	-	-	DC	-	-	DC	-	-	DC	-	Refer to legend

Address	Length (Byte)	Description	ET1200	ET1100	IP Core V3.0.0-V3.0.10, V3.00c-V3.00k			IP Core V2.4.0-V2.4.4/ V2.04a-V2.04e			IP Core V2.3.0-V2.3.2/ V2.03a-V2.03d			IP Core V2.2.1/V2.2.0/ V2.02a			IP Core V2.0.0/V2.00a			IP Core V1.1.1/V1.01b			IP Core V1.1.0			IP Core V1.0.0			ESC20	IP Core Option
					Register set			Register set			Register set			Register set			Register set			Register set			Register set							
					S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L		
0x0E00:0x0E03	4	Power-On Values [Bits]	8	16	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-			
0x0E00:0x0E07	8	Product ID	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-			
0x0E08:0x0E0F	8	Vendor ID	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-			
0x0E10	1	ESC Health Status	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-			
0x0F00:0x0F03	4	Digital I/O Output Data	x	x	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	x	Selected PDI		
0x0F10:0x0F17	8	General Purpose Outputs [Byte]	2	2	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	-	Number of GPIOs		
0x0F18:0x0F1F	8	General Purpose Inputs [Byte]	-	2	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	-	Number of GPIOs		
0x0F80:0x0FFF	128	User RAM	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x				
0x1000:0x1003	4	Digital I/O Input Data	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	Process Data RAM		
0x1000 ff.		Process Data RAM [Kbyte]	1	8	0-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	4	Process Data RAM			

Table 5: ESC Register Legend

Symbol	Description	ET1200 EEPROM setting	ET1100 EEPROM setting	Option IP Core since V3.0.0/V3.00c	Option IP Core V2.2.0/V2.02a-V2.4.4/V2.04e	Option IP Core V2.0.0/V2.00a	Option IP Core V1.0.0-V1.1.1/V1.01b	ESC20
x	Available							
-	Not available							
r	Read only							
c	Configurable							
RT	DC Receive Times enabled	x	x	Receive Times	Receive Times	Distributed clocks	Distributed clocks	x
DC	DC Time Loop Control enabled	x	0x0000[10]=1, or 0x0000[11]=1	Distributed clocks	Distributed clocks	Distributed clocks	Distributed clocks	x
SL	DC SYNC Out Unit and/or Latch In Unit enabled	x	0x0000[10]=1, or 0x0000[11]=1	DC SyncSignals>0, or DC LatchSignals>0	Distributed clocks	Distributed clocks	Distributed clocks	x
S	DC SYNC Out Unit enabled	x	0x0000[10]=1	DC SyncSignals>0	Distributed clocks	Distributed clocks	Distributed clocks	x
S#	DC SYNC Out Unit instance # enabled	x		DC SyncSignals	Distributed clocks	Distributed clocks	Distributed clocks	x
L	DC Latch In Unit enabled	x	0x0000[11]=1	DC LatchSignals>0	Distributed clocks	Distributed clocks	Distributed clocks	x
L#	DC Latch In Unit instance # enabled	x		DC LatchSignals	Distributed clocks	Distributed clocks	Distributed clocks	x
ET	DC SyncManager Event Times are enabled	x	0x0000[10]=1, or 0x0000[11]=1	SyncManager Event Times	SyncManager Event Times	SyncManager Event Times	Distributed clocks	
io	Available if Digital I/O PDI is selected							
red	Register changed in this version							

4 Appendix

4.1 Support and Service

Beckhoff and our partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

4.1.1 Beckhoff's branch offices and representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products!

The addresses of Beckhoff's branch offices and representatives round the world can be found on her internet pages: <http://www.beckhoff.com>

You will also find further documentation for Beckhoff components there.

4.2 Beckhoff Headquarters

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Beckhoff Support

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